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MS-7592

Version 10

CPU:

Intel Conroe (95W Dual core)

System Chipset:

Intel G41 - MCH (North Bridge)

Intel ICH7R (South Bridge)

On Board Chipset:

BIOS -- SPI

HD -- ALC888S

LPC Super I/O -- F718829G

LAN-- REALTEK RTL8111D Co-lay RTL8103E

CLOCK -- RTM875-605

Main Memory:

DDR II *2 (Max 4GB)

Expansion Slots:

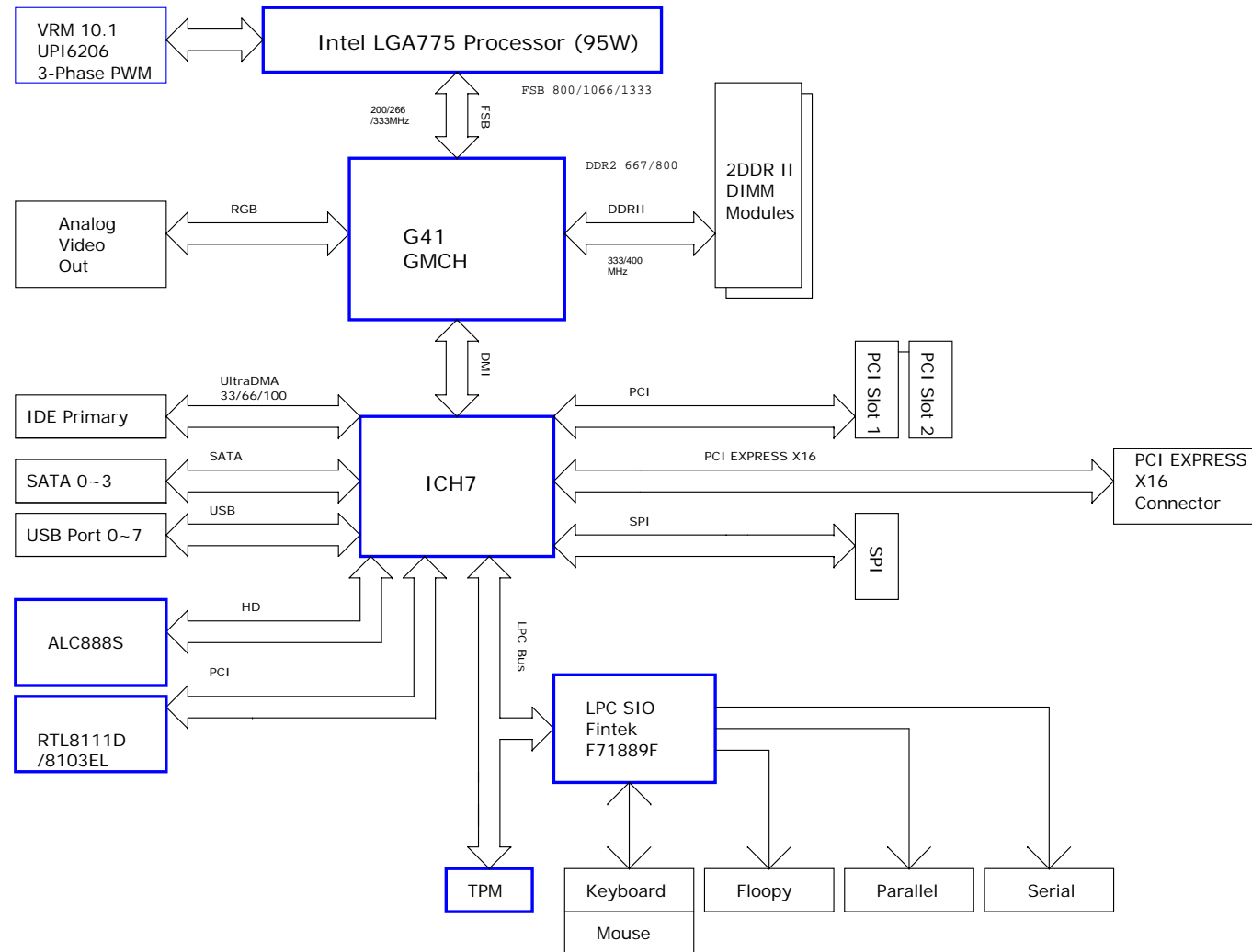
PCI2.3 SLOT * 2

PCI EXPRESS X16 SLOT

ST PWM:

Controller: 3 PHASES

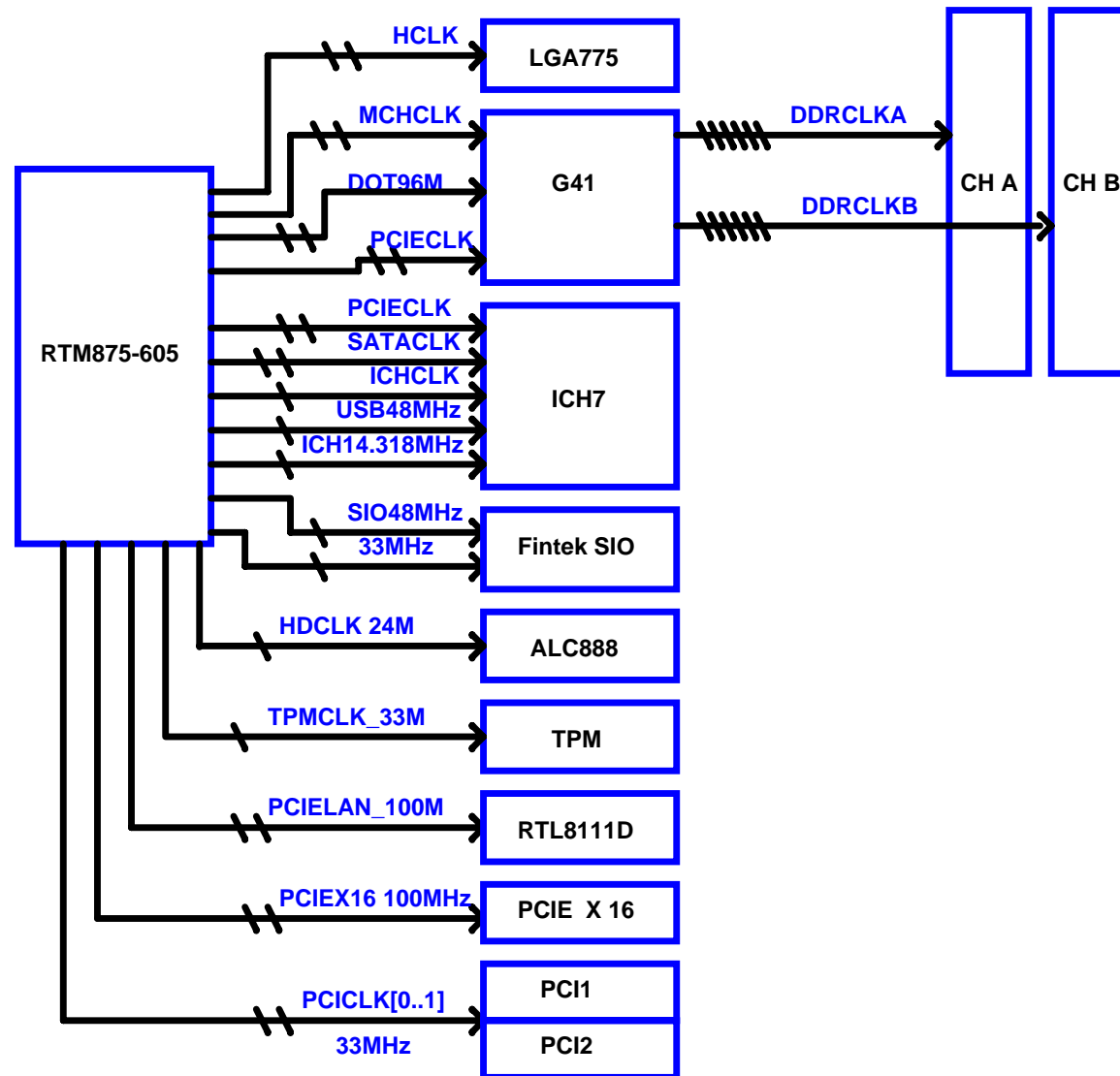
Block Diagram



www.schematic-x.blogspot.com

MICRO-STAR INT'L CO.,LTD		
MS-7592		
Size Custom	Document Description BLOCK DIAGRAM	Rev 1.1
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CLOCK MAP



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Size
Custom

Document Description
CLOCK MAP

Rev
1.1

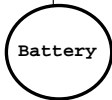
Date: Monday, December 15, 2008

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Processor (95W)
1.15-1.5000V Core-70A
1.2V FSB Vtt-5.8A
VCCPLL
VCC-IOPLL & VCCA

G41 MCH 1.1V core 22A
1.2V FSB Vtt-0.9A
1.8V DDR2 I/O-4.4A(S0,S1)
1.8V DDR2 I/O-25mA(S3)
0.9V DDR2 VREF-2mA
0.9V DDR2 SB_VREF-10uA
DDR2 Resister Comp V-36mA
DDR2 Resis Comp SB_V-10uA
1.1V Core-13.8A(Integrated)
1.1V Core-8.9A(Discrete)
1.5V PCI Express&DMI-0.68A
1.1V PCIE&DMI PLL-41mA
1.5V HOST PLL-45mA
1.5V VCCA_DPLLA&B-55mA
1.5V MPLL-66mA
1.1V Vcc-core 1.16A
1.1V VCC_CL-3A

ICH7
1.2V VCC_CPU-14mA
1.05V Core-0.86A
VCC1_5 SATA/USB/PLL 1.65A
VCC1_5B*-0.646A
5VRef-6mA
5VrefSus-10mA
+3.3V-0.33A
RTC-6uA(G3)
3.3V VccSus*-52mA
VccSus1_05V-See Note 1
VccUSBPLL-10mA
VccDMIPLL-41mA
VccSATAIPLL-50mA



Divider

R

R

L

L

+12V
ATX 2x2

+12V	+5V	+3.3V	+5VSB
ATX POWER			

UPI6206 Regulator
VCCP
1.15-1.5000V

VTT Regulator
V_FSB_VTT
1.2V

uP6103 Regulator
VCC_DDR
1.8V

V1.5 Regulator
V_1P5_CORE
1.5V

1.1V Regulator
V_1P1_Core
1.1V

1.05V Regulator
V_1P05_CORE
1.05V

uP7706 Regulator
3VSB
3.3V

uP7501 Regulator
5VDIMM
5V

W83310DS Regula
VTT_DDR
0.9V

DDR2 DIMM conn(4) & term
0.9V SM Vtt-1.2A(S0)
1.8V Vdd/vddq-4.7A(S0,S1)

PCIE X16 slot(1)
+12V-5.5A
+3.3Vaux-375mA(wake)
+3.3Vaux-20mA(no wake)
+3.3V-3.0A

PCIE X1 slot(0)
+12V-0.5A
+3.3Vaux-375mA(wake)
+3.3Vaux-20mA(no wake)
+3.3V-3.0A

PCI slot slot(2)
+3.3Vaux-375mA(wake)
+3.3Vaux-20mA(no wake)
+3.3V-5.6A
+5.0V-5.0A
+12V-0.5A
-12V-0.1A

USB
+5V-4A(S0,S1)

PS2
+5V-345mA(S0,S1)

CLKGEN
+3.3V-560mA

LAN
3VSB-

SIO
+3.3V
3VSB-

SPI ROM

Audio Codec

1394

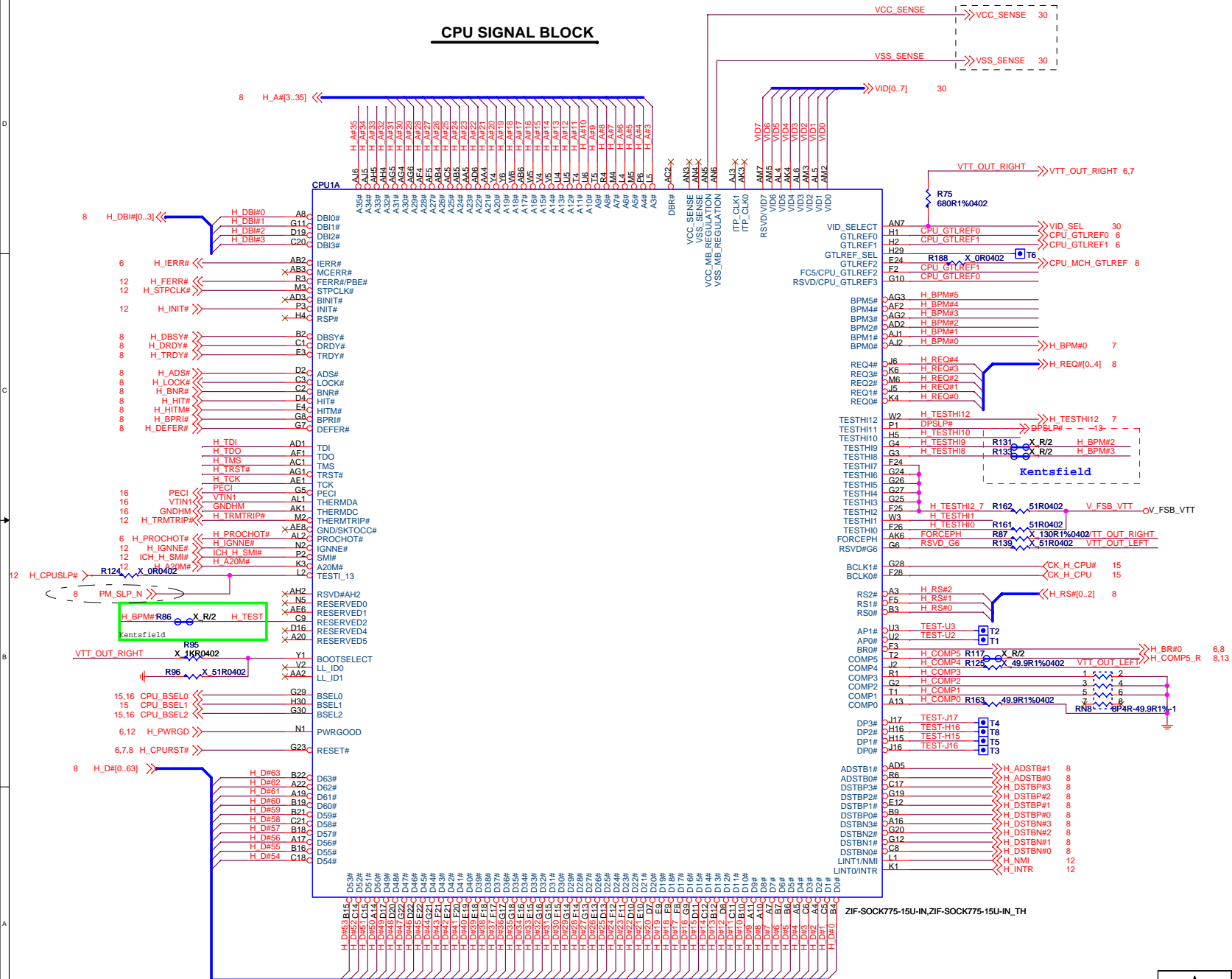


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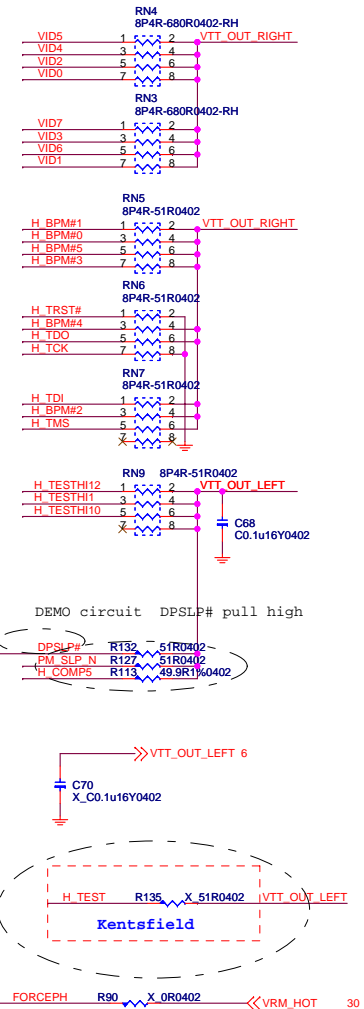
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Size	Document Description	Rev
Custom	LG4775 - Signal	1.1
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CPU SIGNAL BLOCK



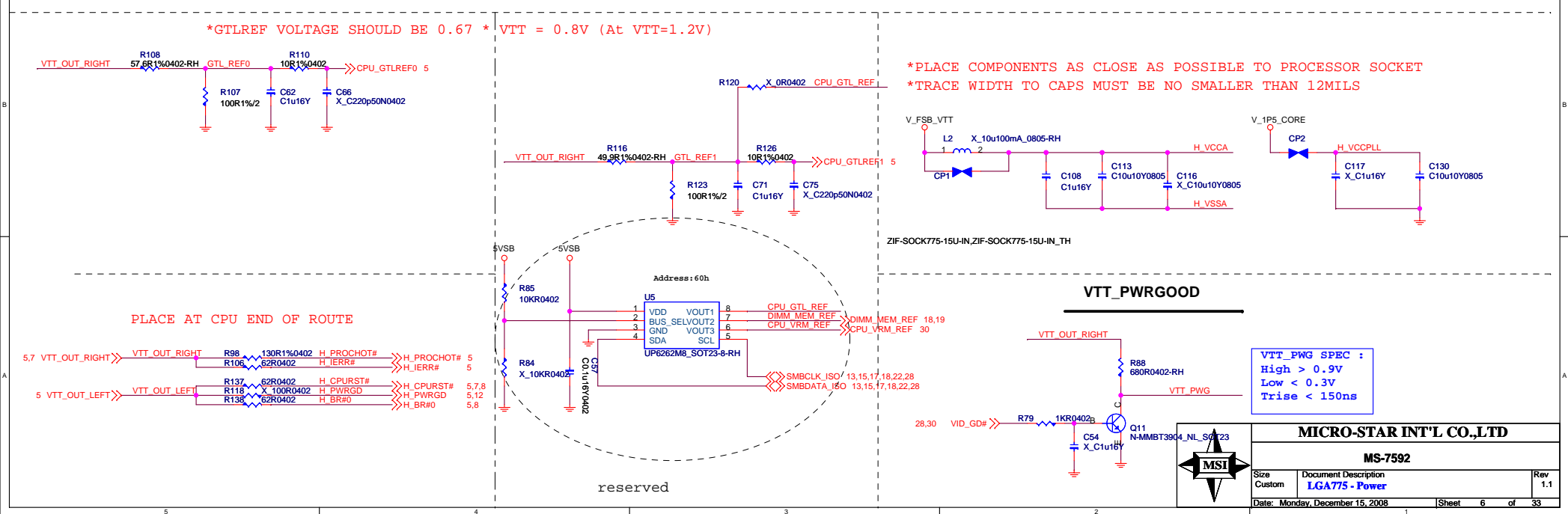
PULL HIGHT PULL DOWN

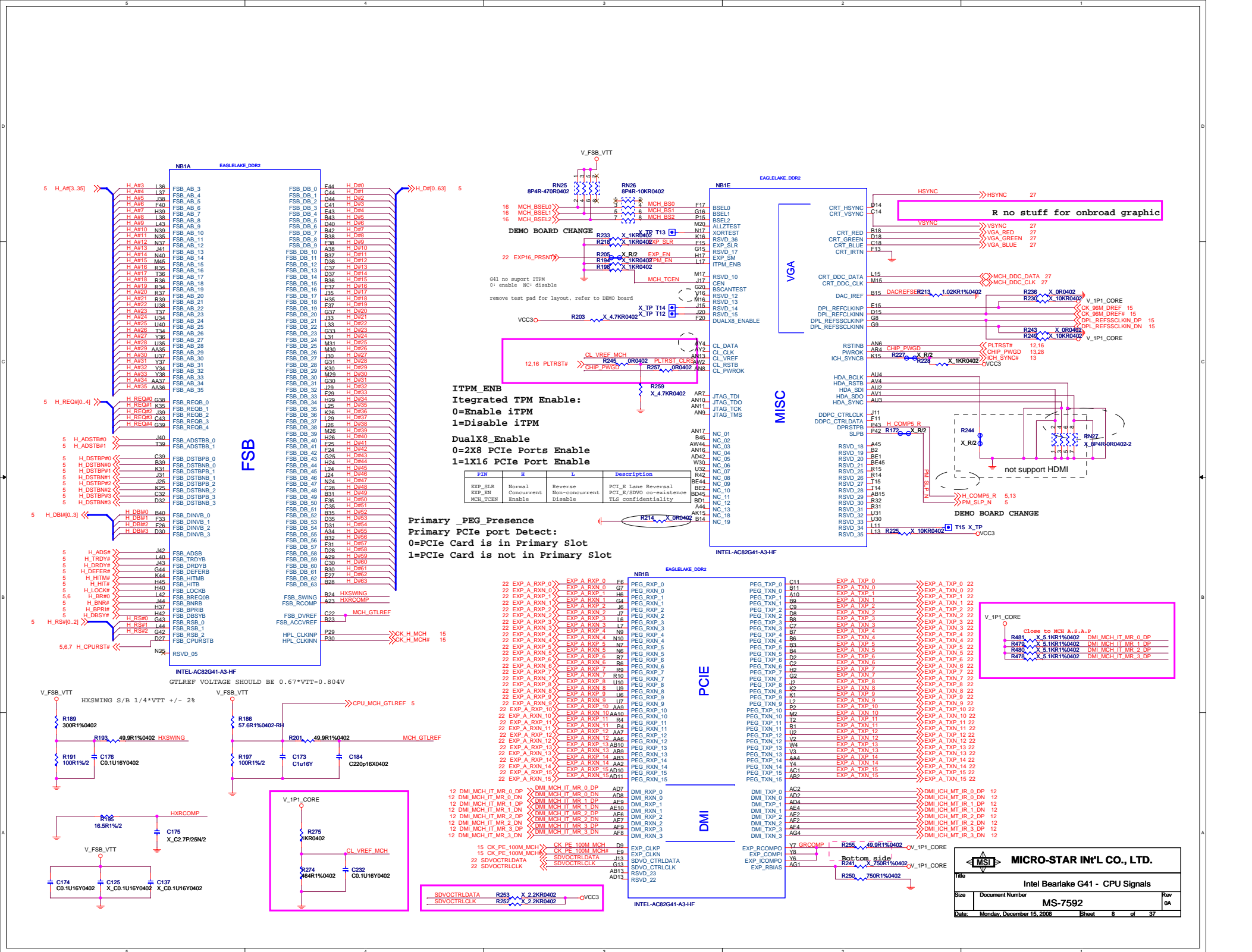


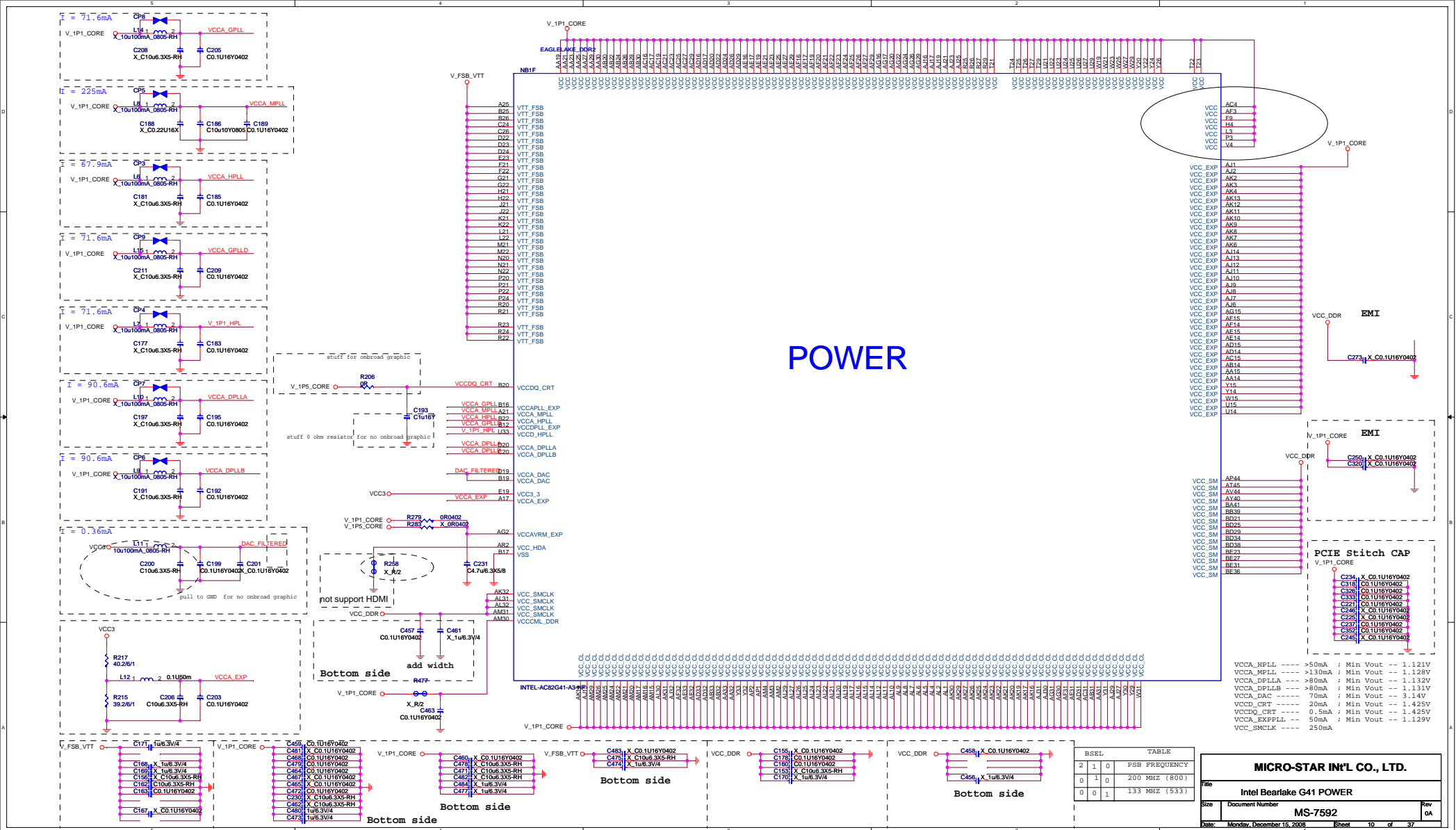
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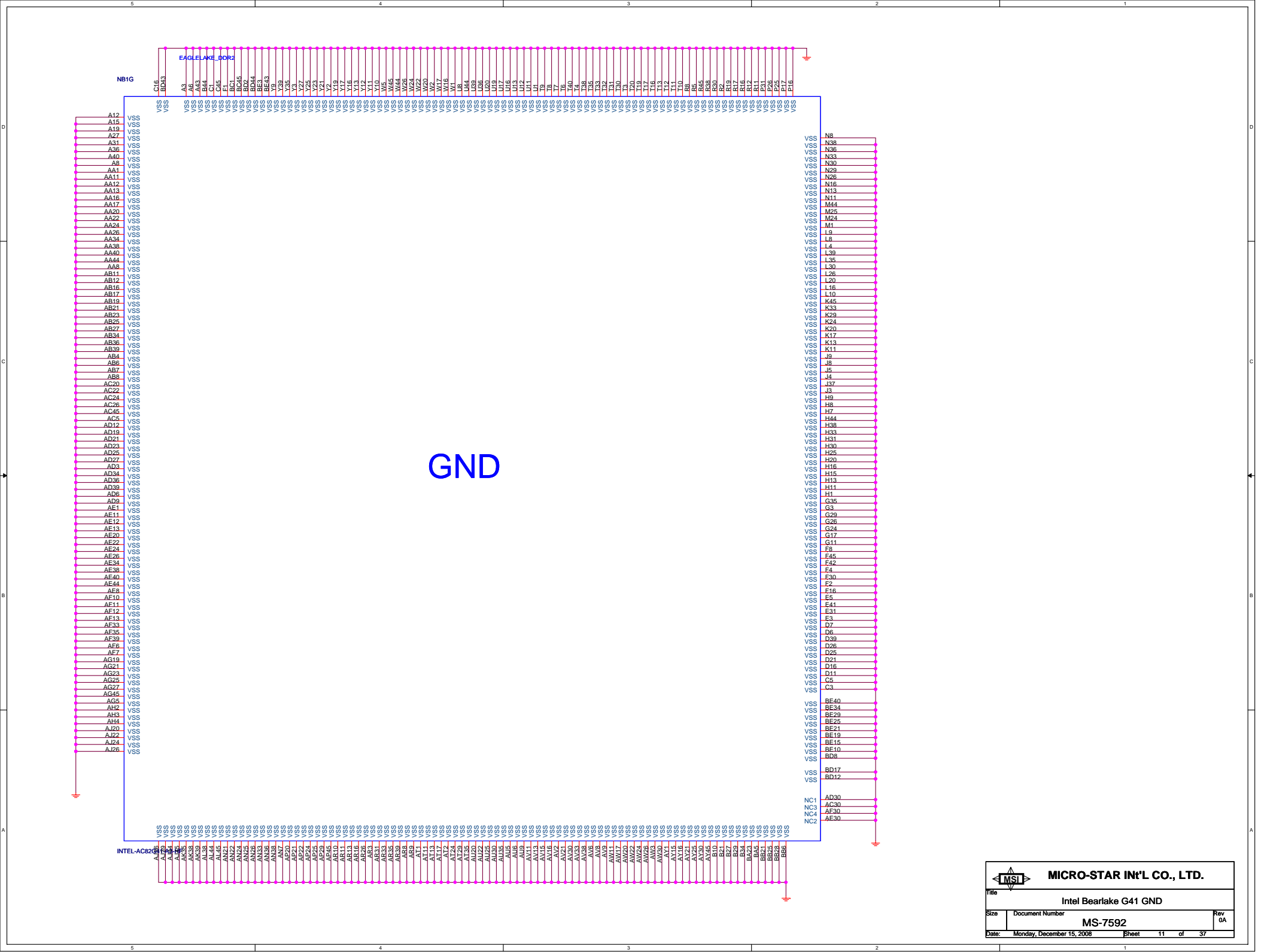
MS-7592

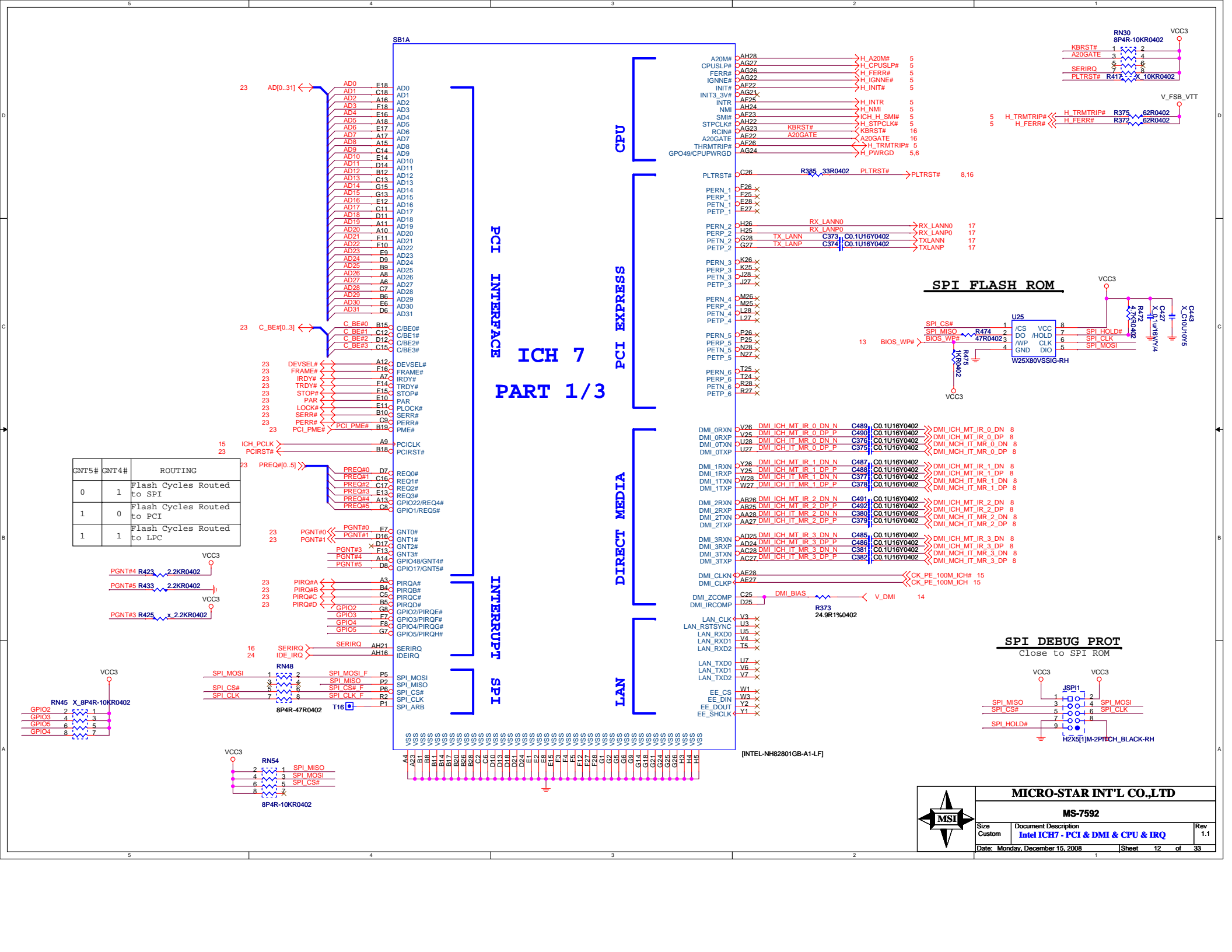
Size Custom	Document Description LGA775 - Signal	Rev 1.1
Date: Monday, December 15, 2008		Sheet 5 of 33

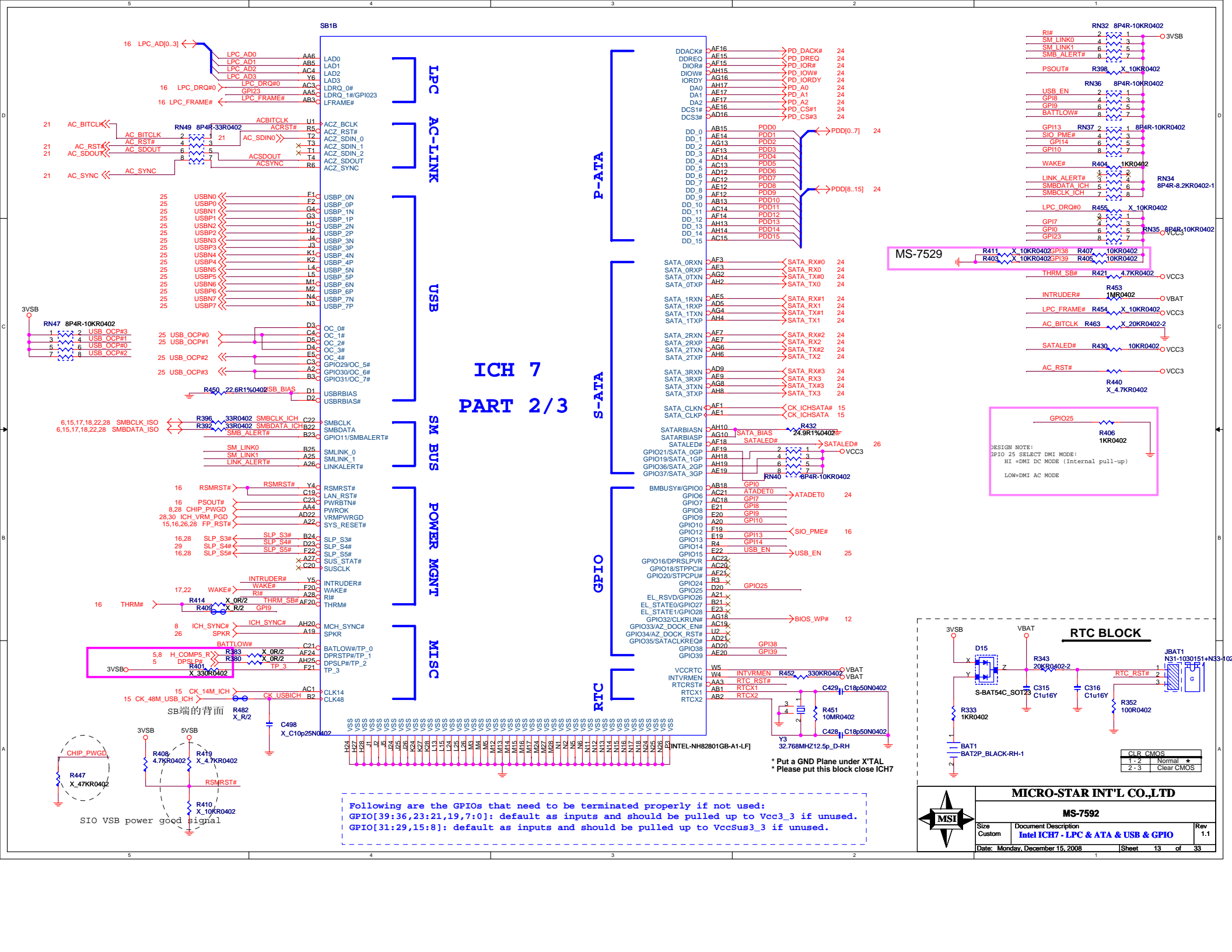






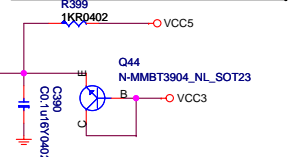






ICH 7
PART 3/3

5VREF Sequencing Circuit



1.5V DMI POWER

S0 POWER

S5 POWER

1.5V CORE WELL POWER

[INTEL-NH82801GB-A1-LF]

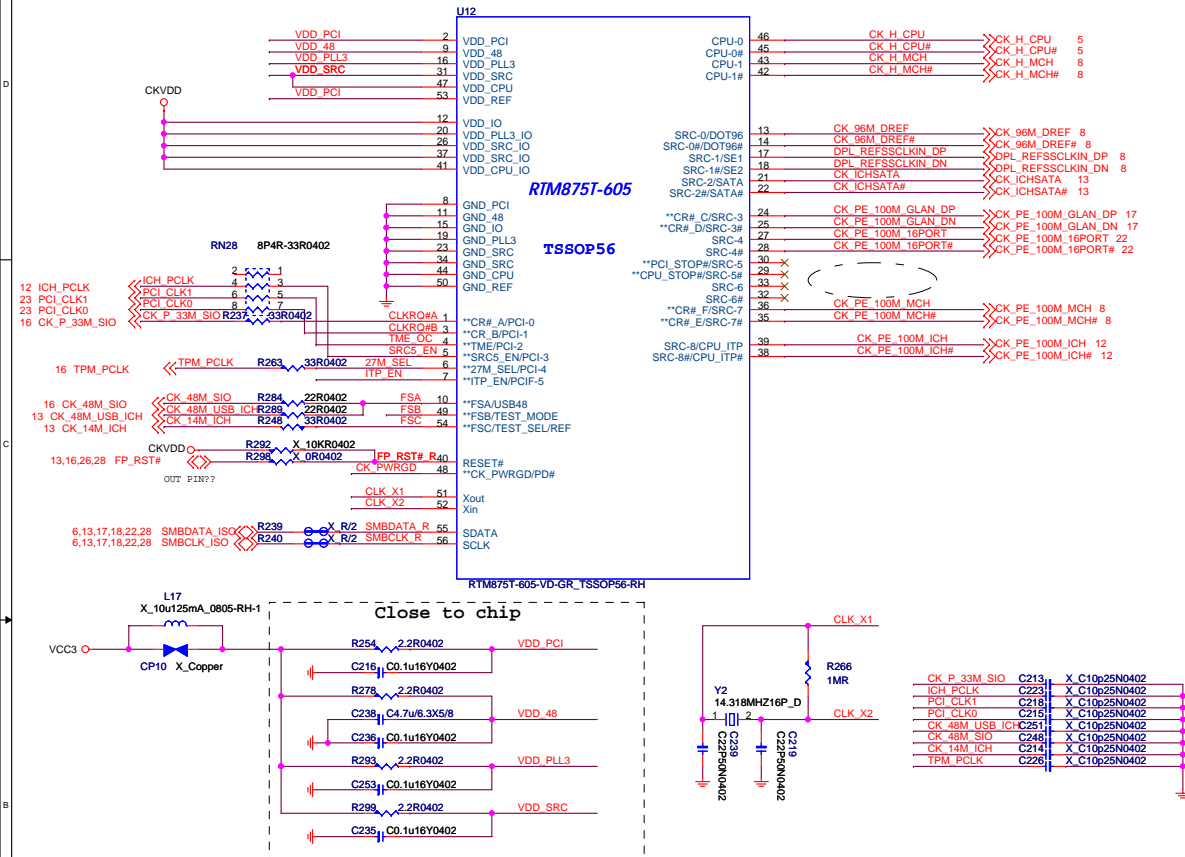


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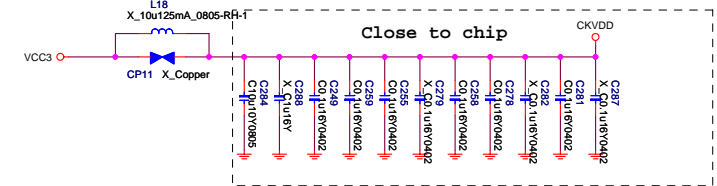
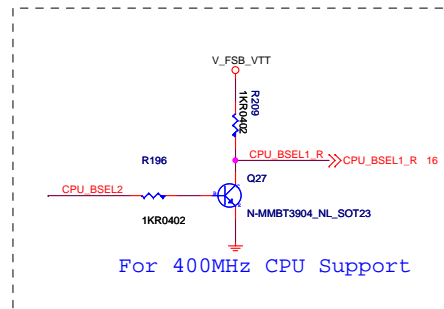
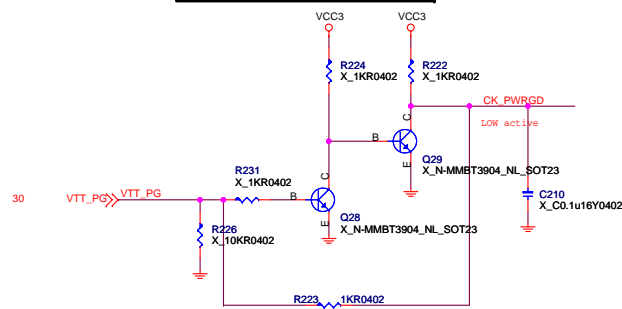
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Size	Document Description	Rev
Custom	Intel ICH7 - POWER	1.1
Date: Monday, December 15, 2008		Sheet 14 of 33

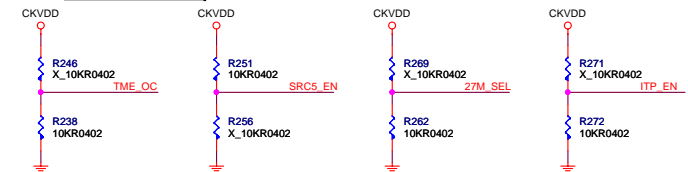
Clock Generator - RTM875T-605



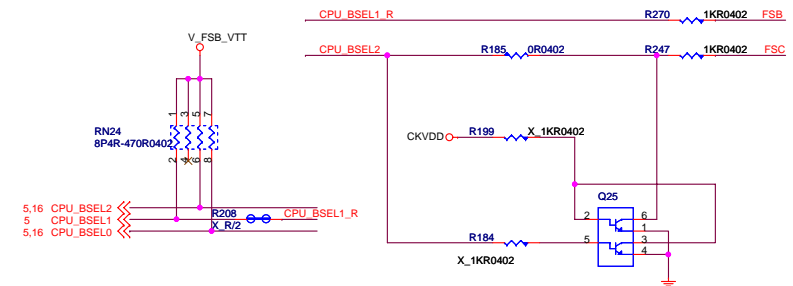
Clock Generator Power Good Block



STRAPPING RESISTOR



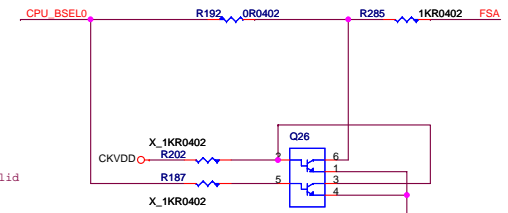
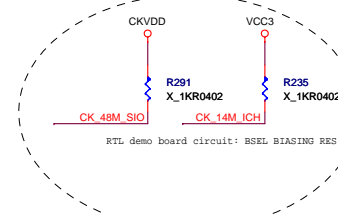
	0	1
TME_OC	Normal Run	No Overclocking
SRC5_EN	Pin29/30 is PCI STOP/CPU STOP	Pin29/30 is SRC 5
27M_SEL	Pin17/18 is SRC 1	Pin17/18 is 27MHz
UTP_EN	Pin38/39 is SRC 8	Pin38/39 is CPUITP



CPU Frequency Selection

FS_C	FS_B	FS_A	CPU
0	0	1	133M
0	1	0	200M
0	0	0	266M
1	0	0	333M
1	1	0	400M

Only the selection in the table is valid

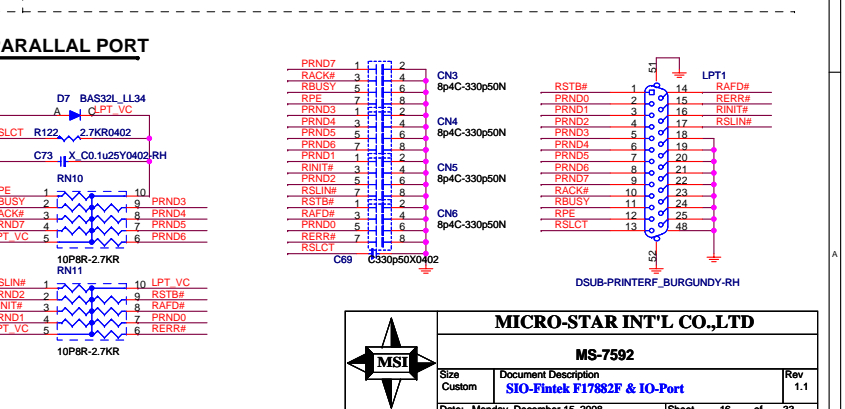
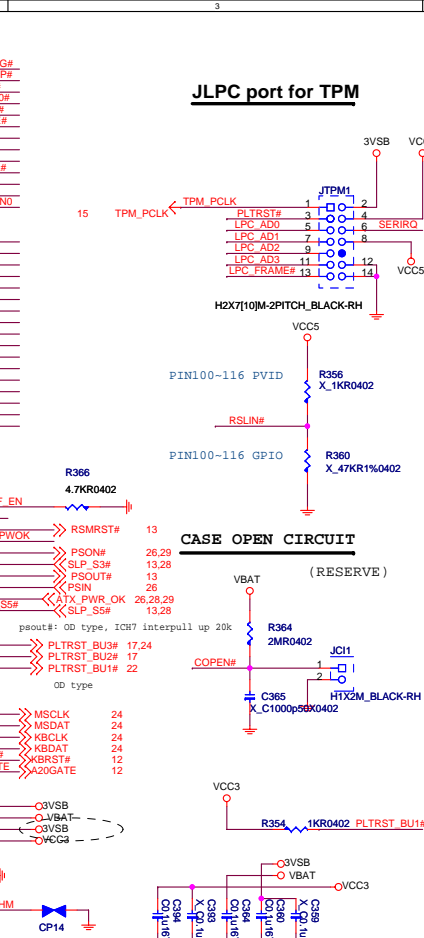


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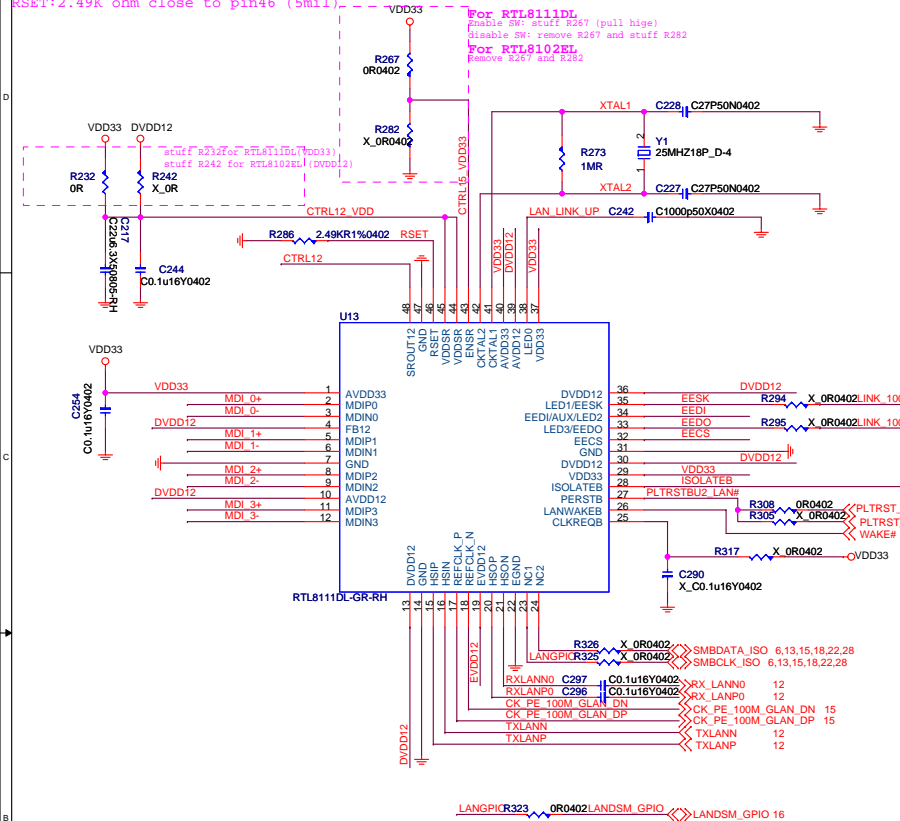
MS-7592

Size Custom	Document Description CLK-RTM 875T-605
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Date: Monday, December 15, 2008	Sheet 15 of 37
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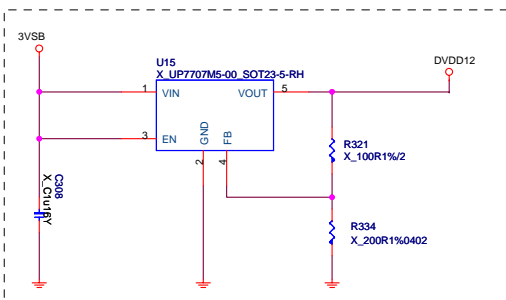


RSET:2.49K ohm close to pin46 (5mil)

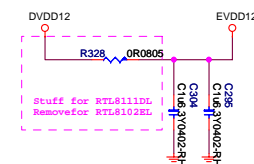
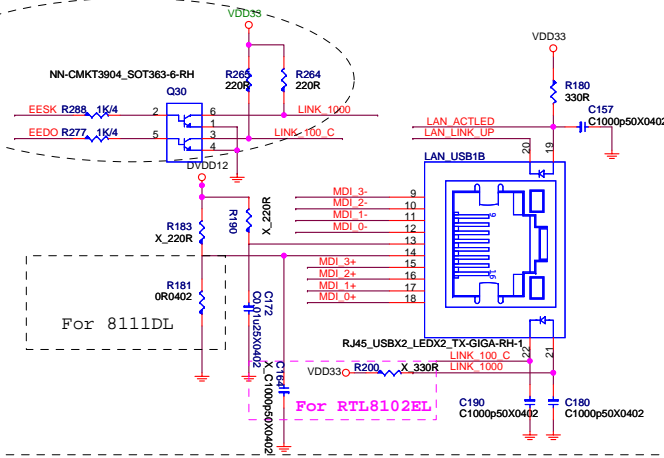
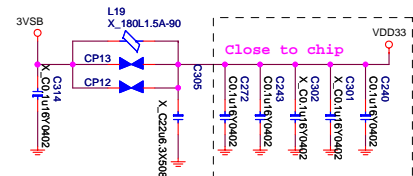
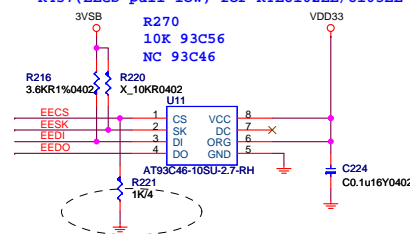


LANGPICR323 OR0402 LANDSM_GPIO LANDSM_GPIO 16

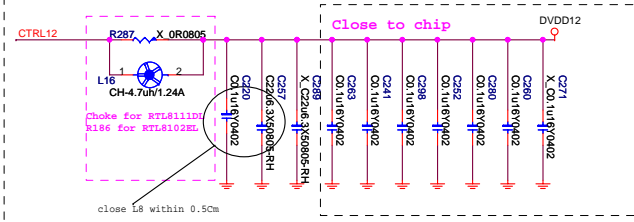
Pin 23 is GPIO pin for 8111DL. It is used for DSM function.



R457(EPCS pull low) for RTL8102EL/8103EL



As close as possible to Pin1 within 500mils



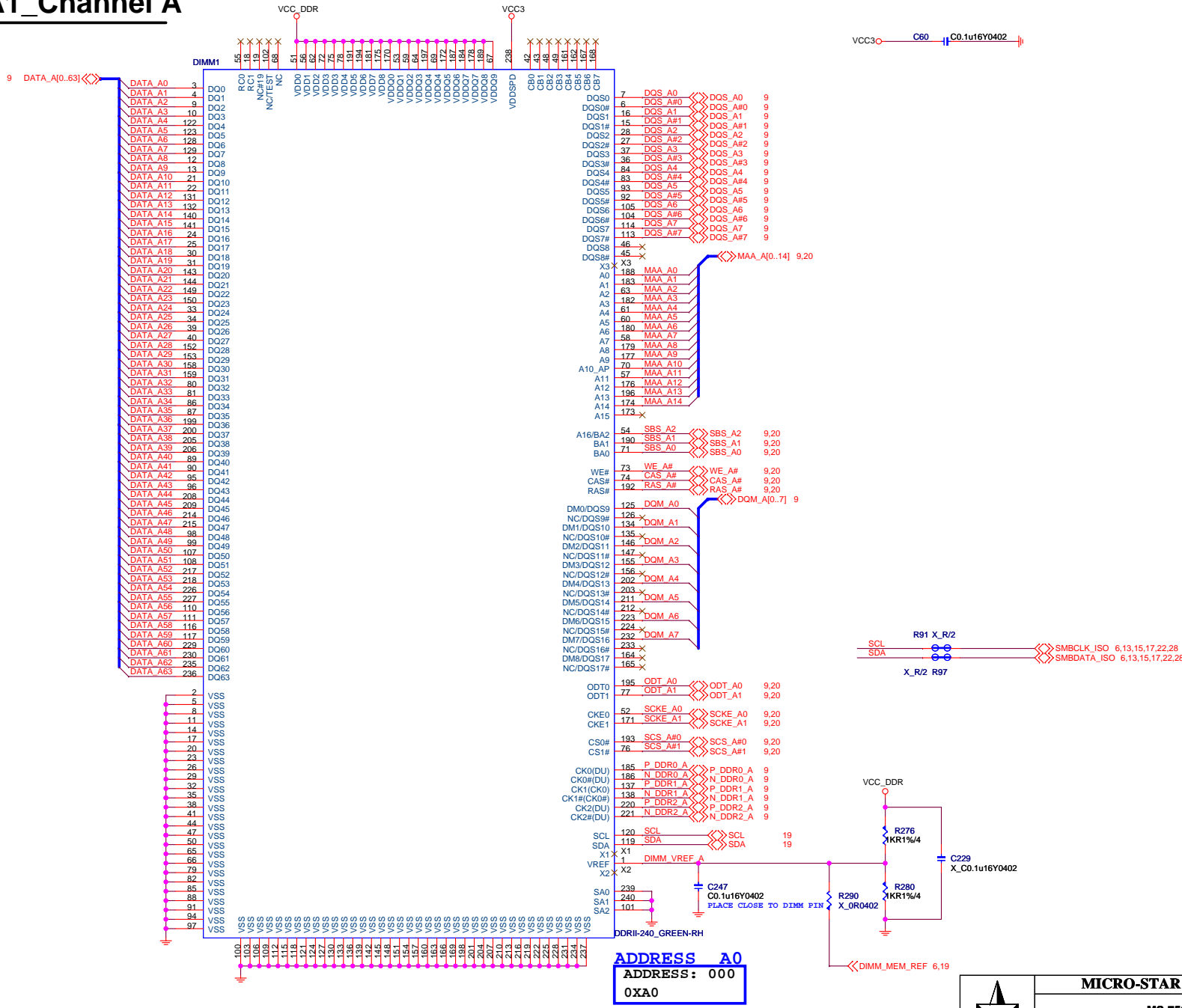
Giga-Lan	10/100-Lan
N58-22F0731-F02	N58-22F0771-F02
Link Yellow	Link Yellow
Active Blinking	Active Blinking
1000 Orange	100 Green
100 Green	10 None
10 None	10 None
19	19
20	20
21	21
22	22

R901 R RTL8103 R902 R 10/100 LAN CONN


RTL8103E : P/N B06-8103E04-R09

Micro Star Restricted Secret		
Title	MS-7592	Rev
Document Number	RTL8111DL/8102EL	0A
MICRO-STAR INT'L CO., LTD.		Last Revision Date:
No. 68, U-De St, Jung-Ho City,		Monday, December 15, 2008
Taipei Hsien, Taiwan		Sheet
http://www.msi.com.tw		17 of 37

DDR II DIMM_A1_Channel A



ADDRESS A0
ADDRESS: 000
0XA0

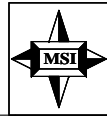
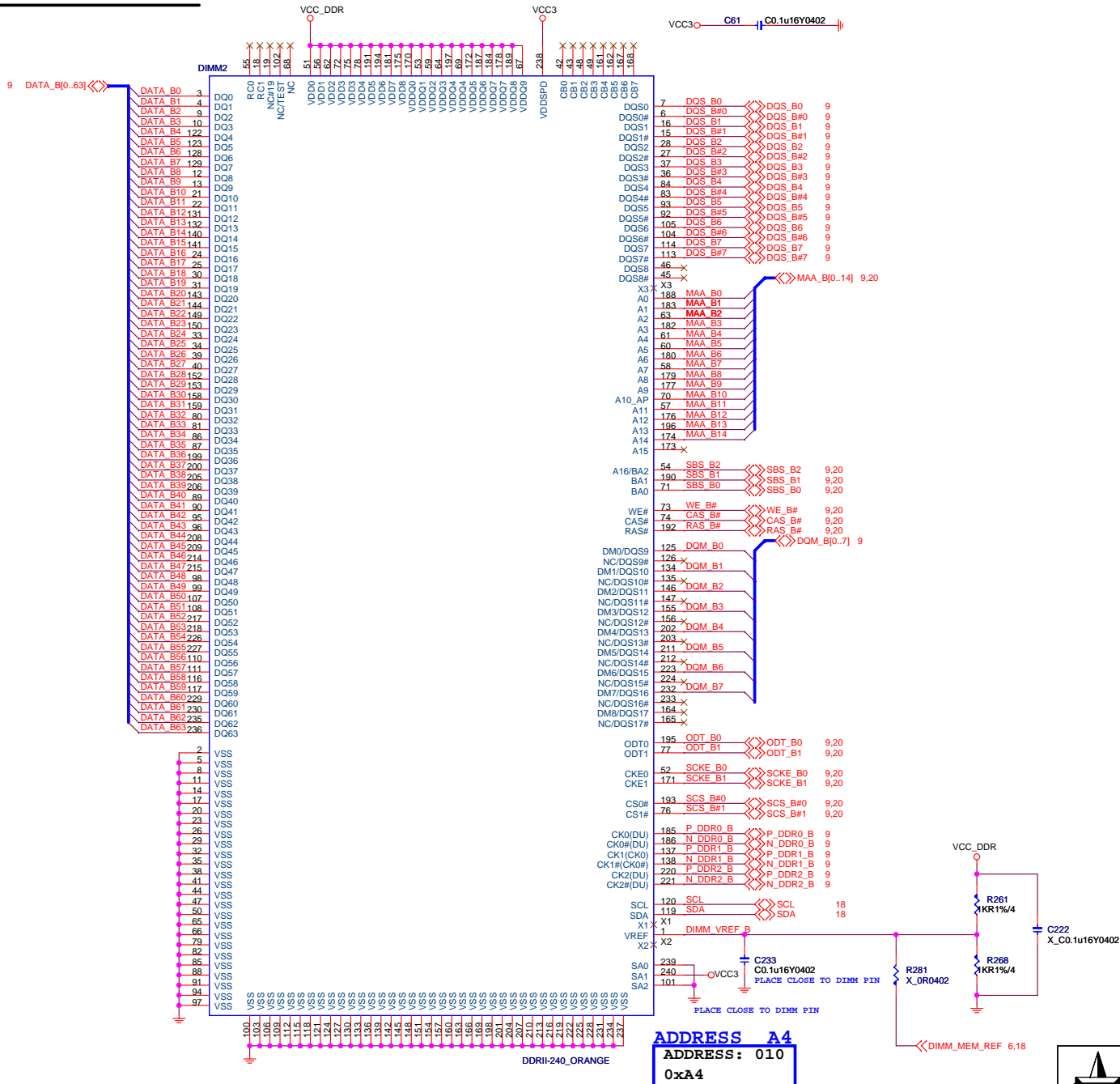


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Size	Document Description	Rev
Custom	DDR II DIMM A	1.0
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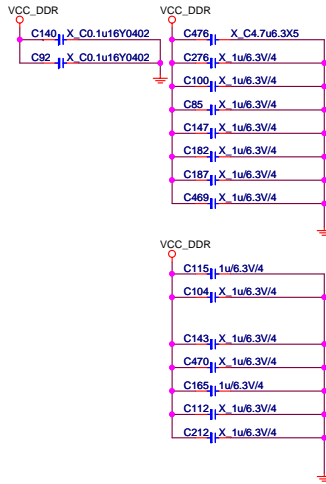
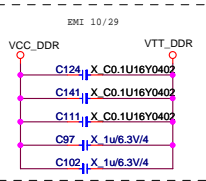
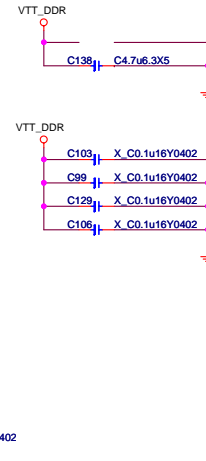
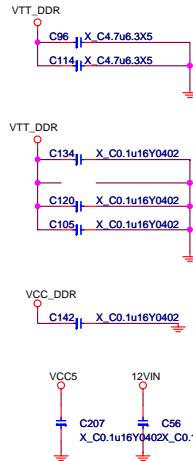
DDR II DIMM_B1_Channel B



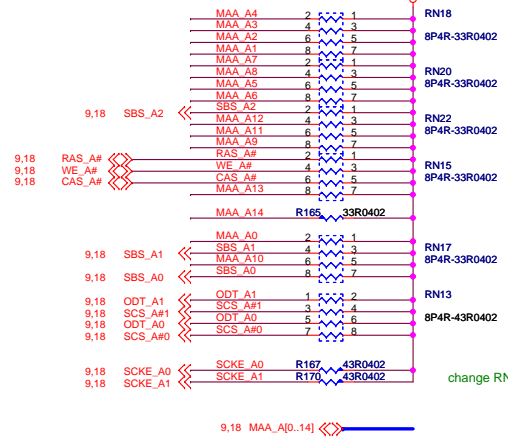
MICRO-STAR INT'L CO.,LTD			
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Size	Document Description	Rev	
Custom	DDR II DIMM B	1.0	
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CHANNEL A V_SM_VTT DECOUPLING CAPS

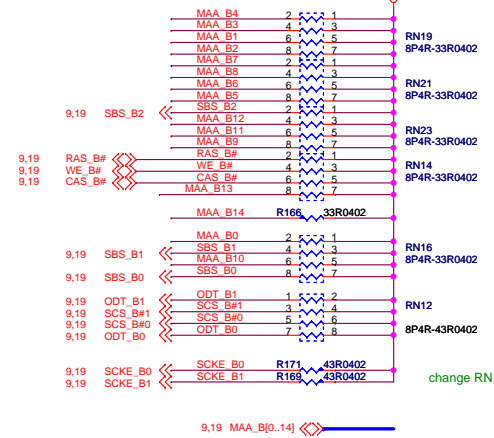
CHANNEL B V_SM_VTT DECOUPLING CAPS



VTT_DDR



VTT_DDR

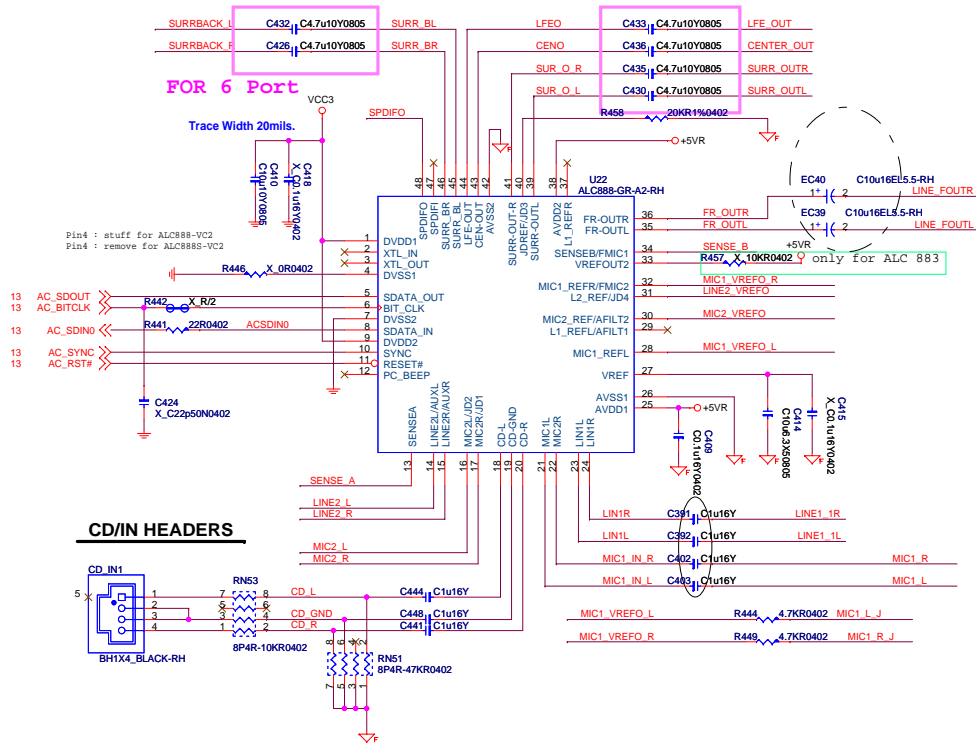


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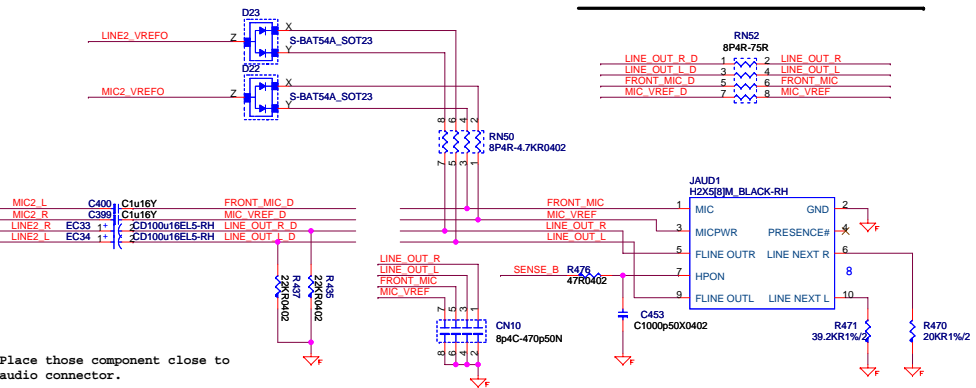
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Size Custom	Document Description DDR II VTT DECOUPLING	Rev 1.0
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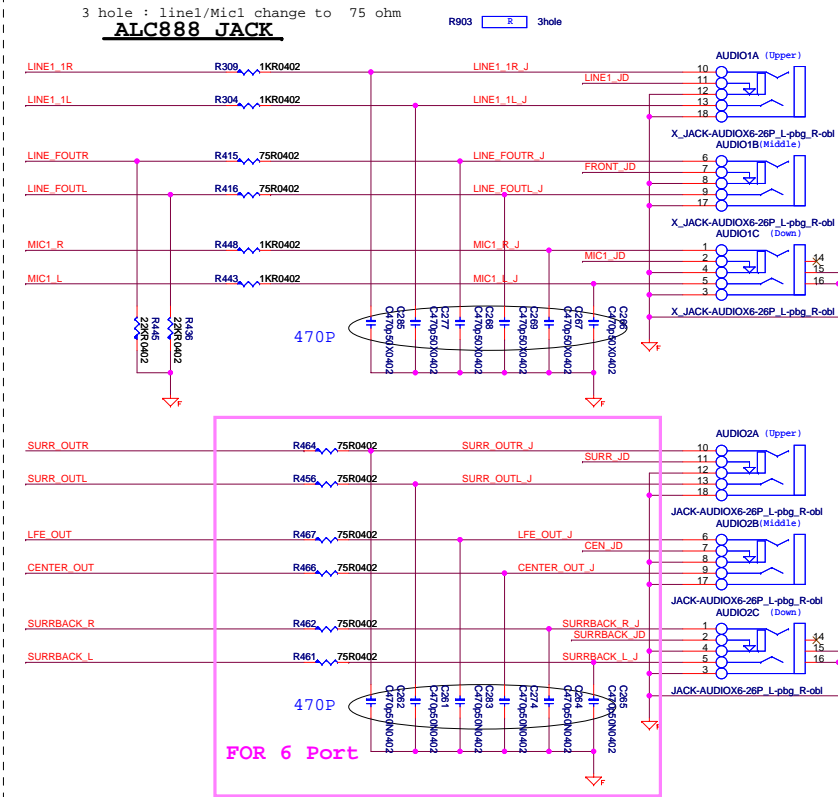
ALC888 CODEC



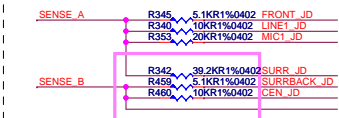
Azalia Front Audio Connector



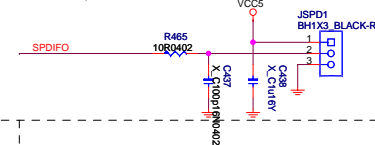
ALC888 JACK



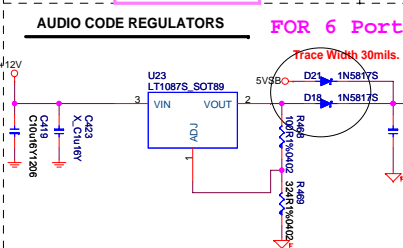
ALC883 JACK DETECT



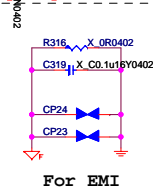
SPDIF OUT



AUDIO CODE REGULATORS



FOR 6 Port

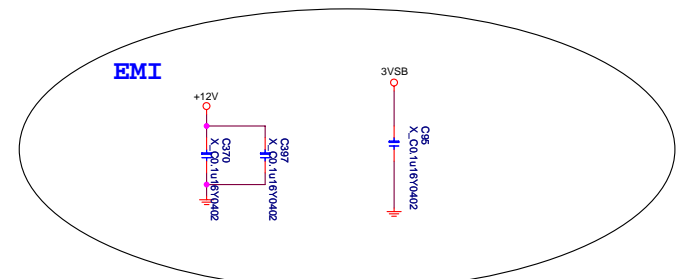
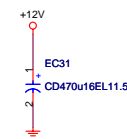
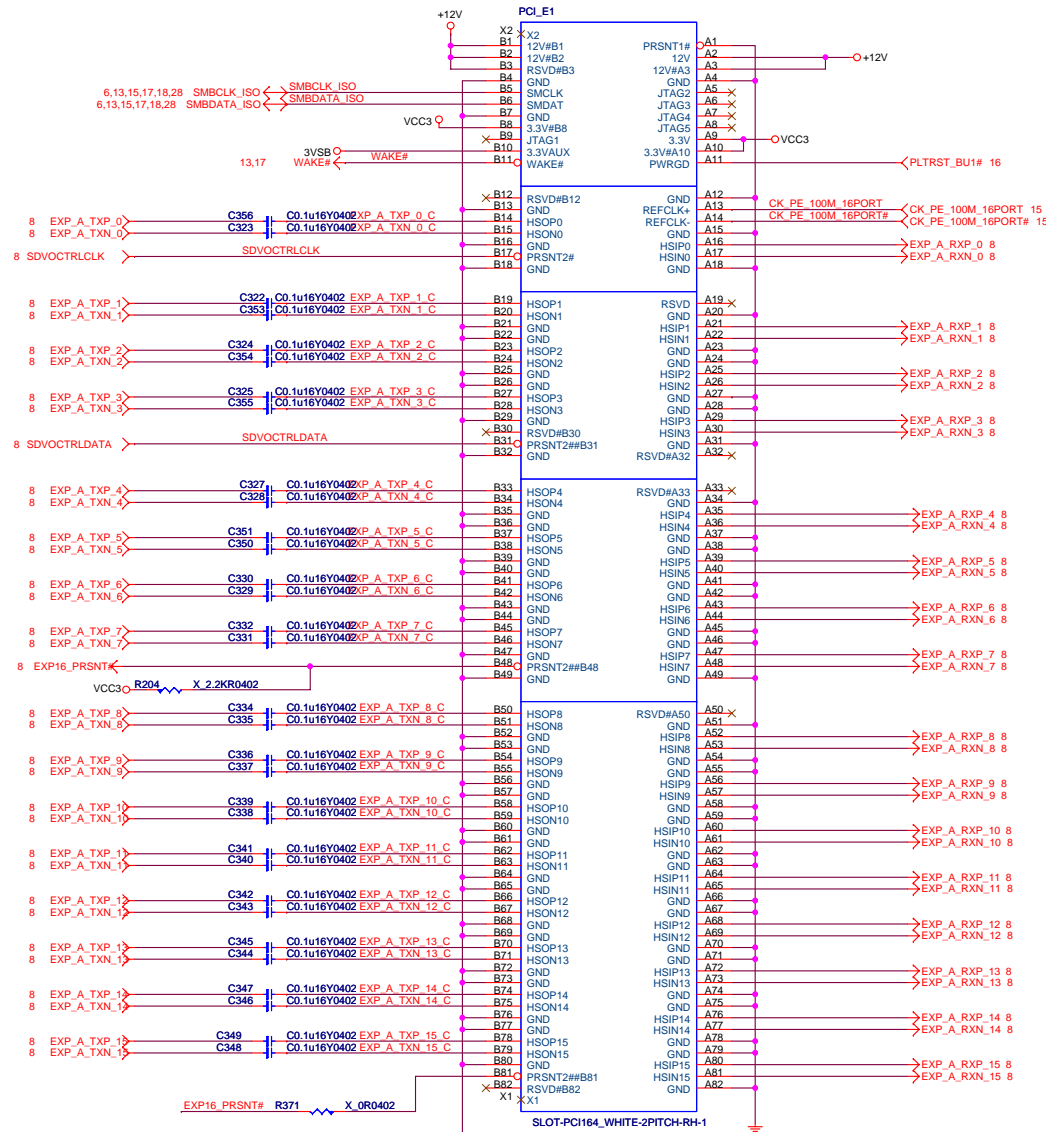


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PCIE X16 PORT

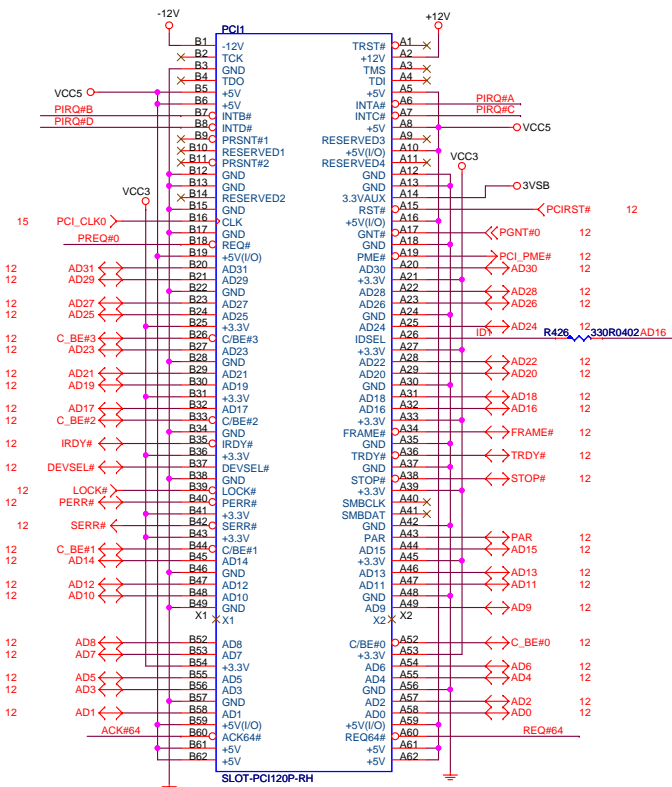


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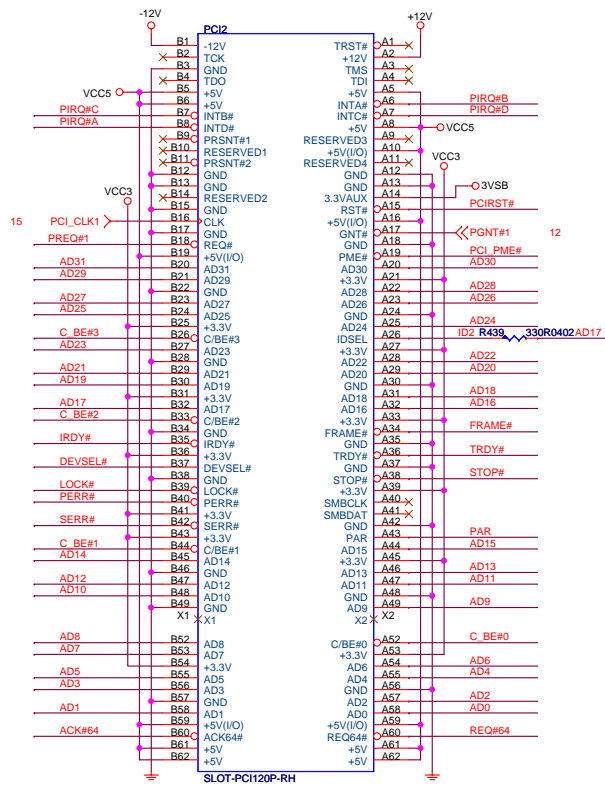
Size	Document Description	Rev
Custom	PCI EXPRESSX16&X1	1.1
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PCI SLOT 1 (PCI VER: 2.2 COMPLY)



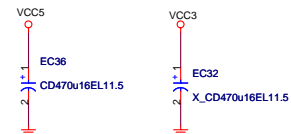
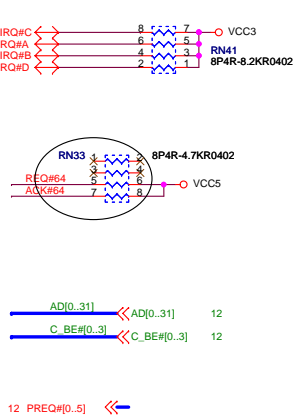
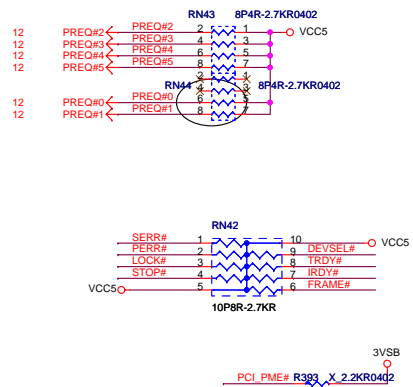
IDSEL = AD16
MASTER = PREQ#0
PIRQ#A

PCI SLOT 2 (PCI VER: 2.2 COMPLY)



IDSEL = AD17
MASTER = PREQ#1
PIRQ#B

PCI PULL-UP / DOWN RESISTORS

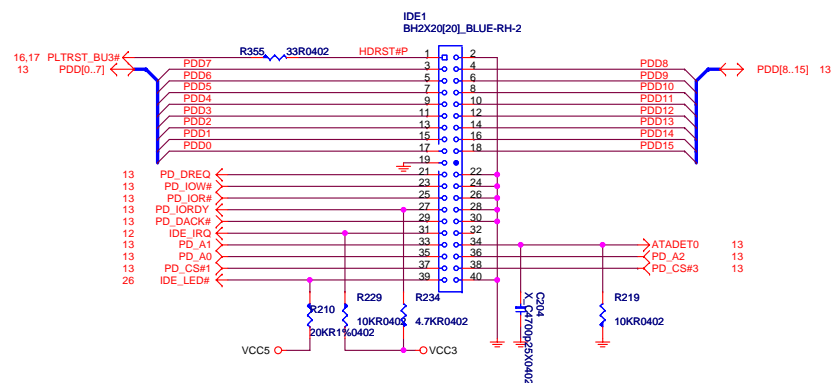


MICRO-STAR INT'L CO.,LTD

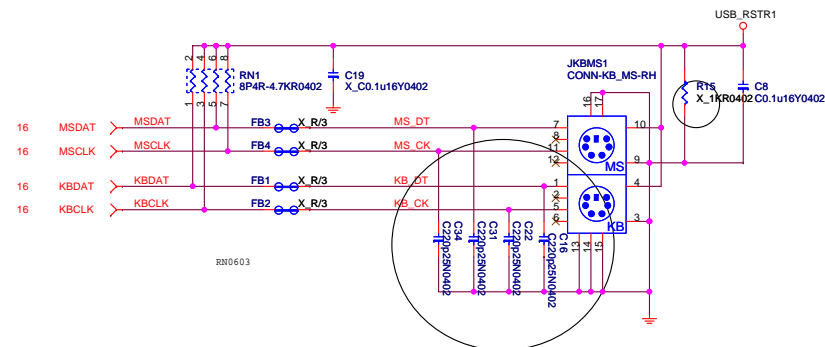
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Size	Document Description	Rev
Custom	PCI Slot 1 & 2	1.1
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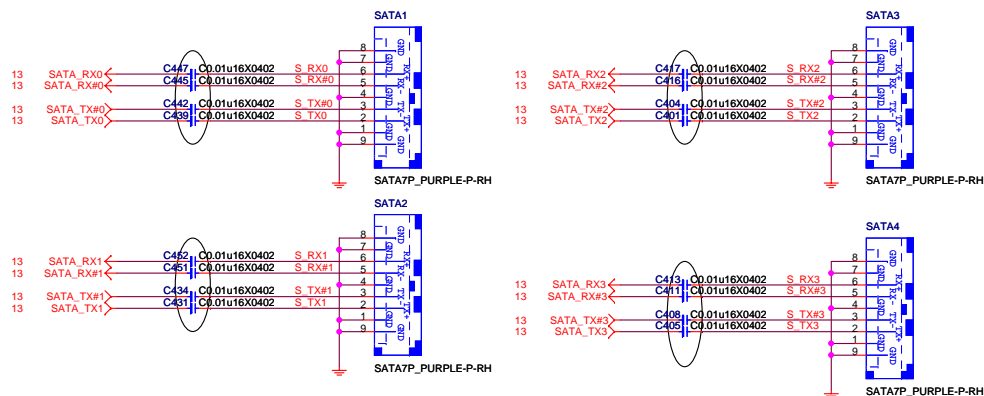
ATA 33/66/100 IDE Connectors



PS2 KEYBOARD & MOUSE CONNECTOR



SERIAL ATA CONNECTOR BLOCK

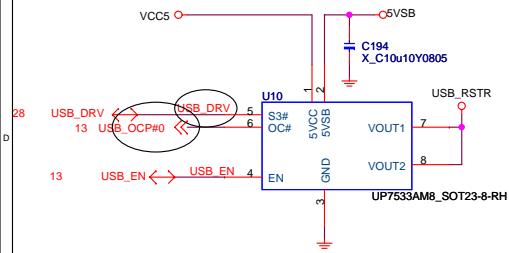


MICRO-STAR INT'L CO.,LTD

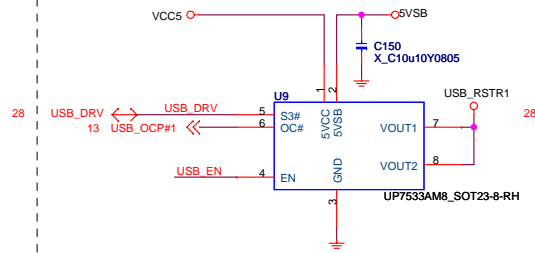
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Size Custom	Document Description IDE & SATA Connectors	Rev 1.1
Date: Monday, December 15, 2008		Sheet 24 of 33

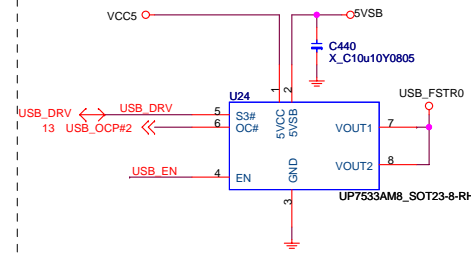
POWER CIRCUIT FOR USB PORT 0,1



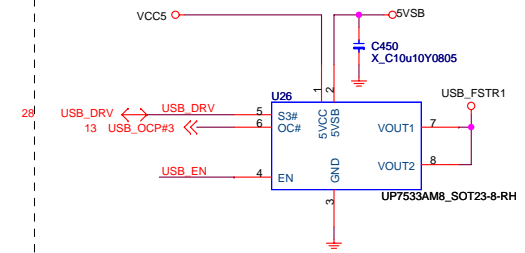
POWER CIRCUIT FOR USB PORT 2,3



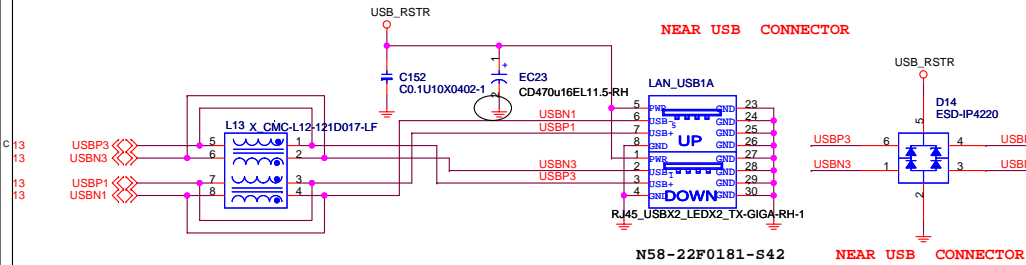
POWER CIRCUIT FOR USB PORT 4,5



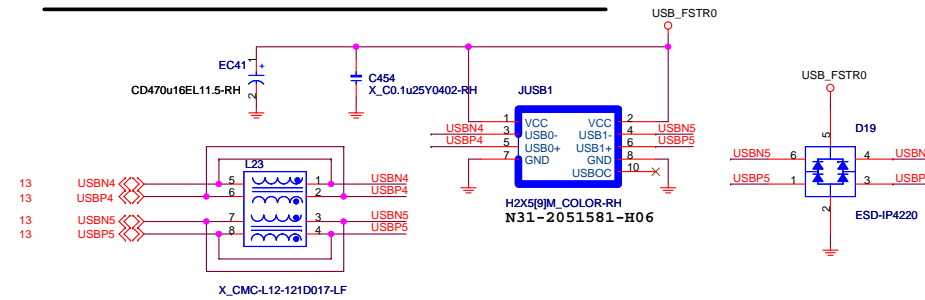
POWER CIRCUIT FOR USB PORT 6,7



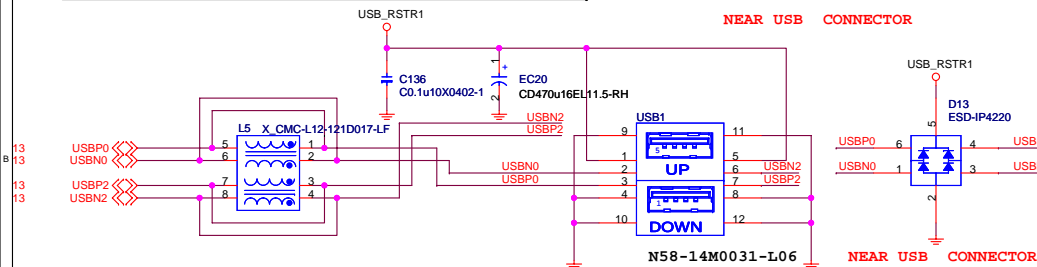
REAR PANEL USB CONNECTOR FOR USB PORT 0,1



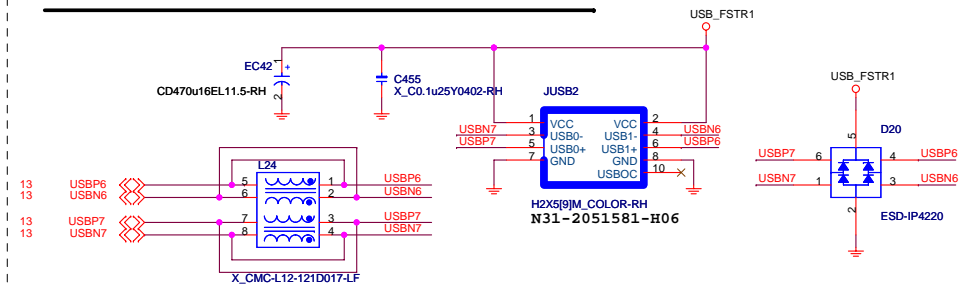
FRONT PANEL USB CONNECTOR FOR USB PORT 4,5



REAR PANEL USB CONNECTOR FOR USB PORT 2,3



FRONT PANEL USB CONNECTOR FOR USB PORT 6,7

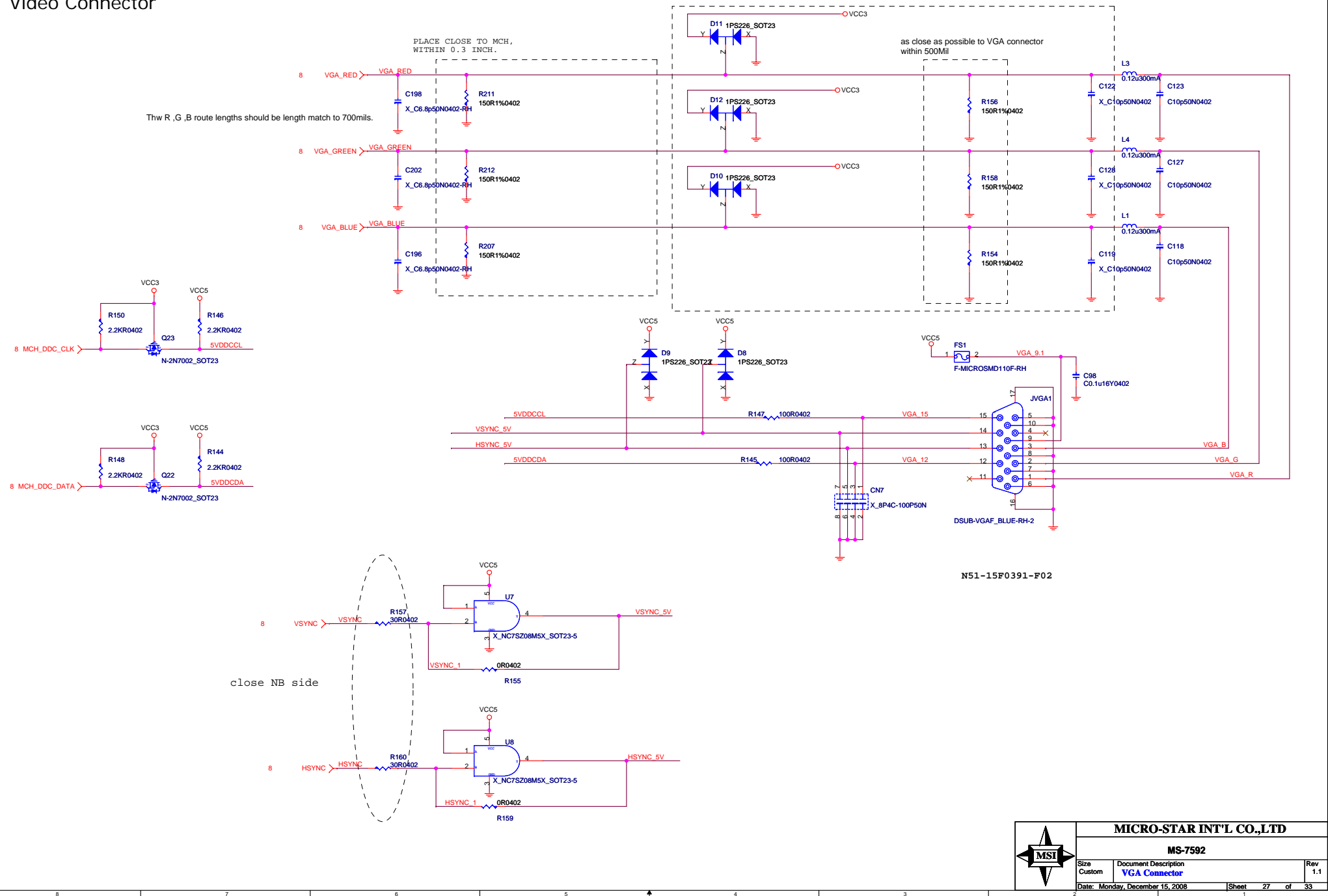


MICRO-STAR INT'L CO.,LTD

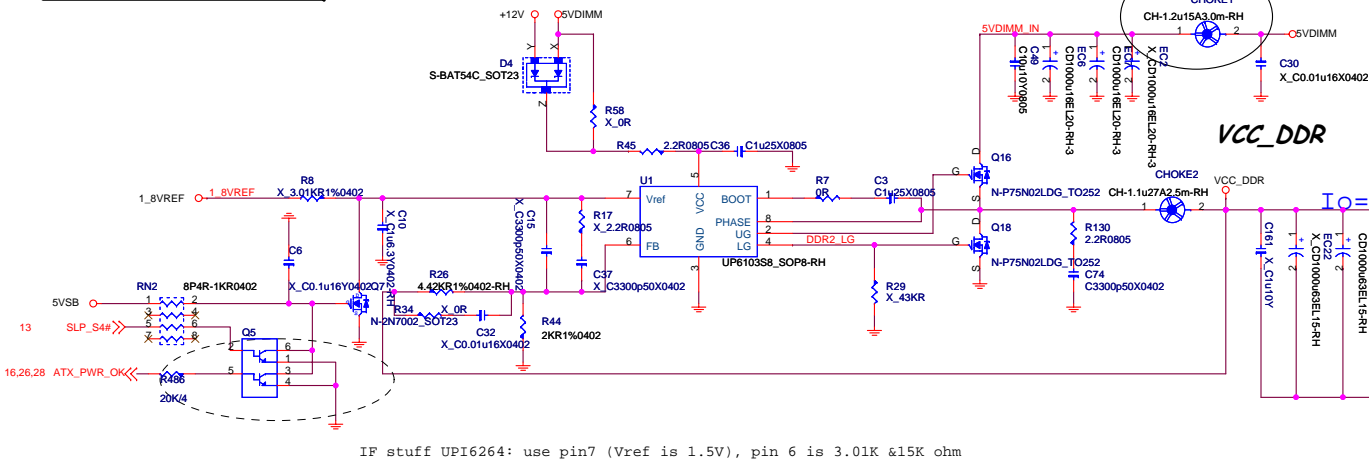
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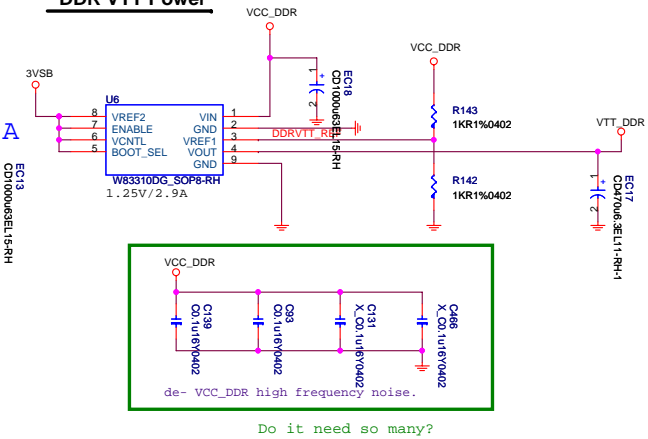
Video Connector



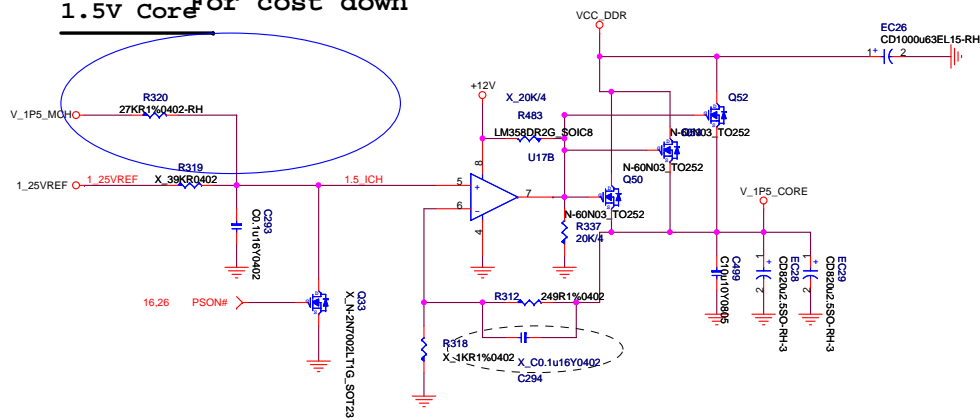
DDR II 1.8V POWER



DDR VTT Power

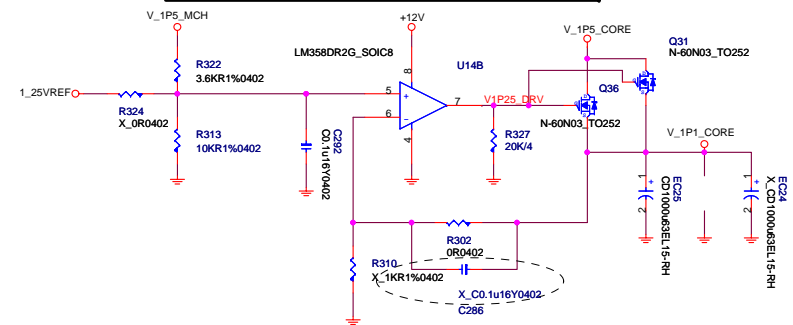


1.5V Core For cost down



? value=> 1.1V 1.5V=> 1.1V 3.6K /10K

V_1P1_CORE 18.1A+2.47A+2.94A

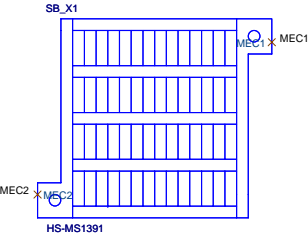


MICRO-STAR INT'L CO.,LTD

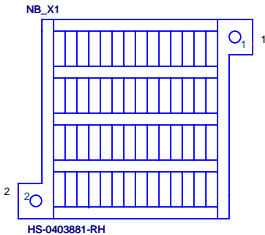
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ICH7 HEATSINK

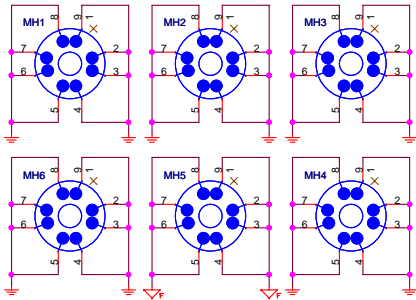


MCH HEATSINK

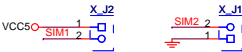


P80-075920A-E48
P80-075920A-G37

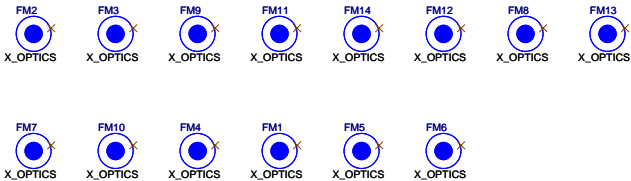
Mounting Holes



Simulation



Optics Orientation Holes



ICH7									
GPIO	Alt Func	PIN	I/O/NC	POWER	PU	SMI	TOL	DEFAULT	SIGNAL NAME
GPIO0	Unmultiplexed	AB18	I/O	CORE	N	Y	3.3V	GPI	GPIO(pull high)
GPIO1	REQ5#	C8	I/O	CORE	N	Y	5V	GPI	PREQ#5
GPIO2	PIRQE#	G8	I/OD	CORE	N	Y	5V	GPI	GPIO2(pull high)
GPIO3	PIRQF#	F7	I/OD	CORE	N	Y	5V	GPI	GPIO3(pull high)
GPIO4	PIRQG#	F8	I/OD	CORE	N	Y	5V	GPI	GPIO4(pull high)
GPIO5	PIRQH#	G7	I/OD	CORE	N	Y	5V	GPI	GPIO5(pull high)
GPIO6	Unmultiplexed	AC21	I/O	CORE	N	Y	3.3V	GPI	ATADET0
GPIO7	Unmultiplexed	AC18	I/O	CORE	N	Y	3.3V	GPI	STRAPPED HI
GPIO8	Unmultiplexed	E21	I/O	Resume	N	Y	3.3V	GPI	STRAPPED HI
GPIO9	Unmultiplexed	E20	I/O	Resume	N	Y	3.3V	GPI	STRAPPED HI
GPIO10	Unmultiplexed	A20	I/O	Resume	N	Y	3.3V	GPI	STRAPPED HI
GPIO11	SMBALERT#	B23	I/O	Resume	N	Y	3.3V	Native	STRAPPED HI
GPIO12	Unmultiplexed	F19	I/O	Resume	N	Y	3.3V	GPI	SIO_PME#
GPIO13	Unmultiplexed	E19	I/O	Resume	N	Y	3.3V	GPI	STRAPPED HI
GPIO14	Unmultiplexed	R4	I/O	Resume	N	Y	3.3V	GPI	STRAPPED HI
GPIO15	Unmultiplexed	E22	I/O	Resume	N	Y	3.3V	GPI	STRAPPED HI
GPIO16	Unmultiplexed	AC22	I/O	CORE	N	N	3.3V	GPO	NC
GPIO17	GNT5#	D8	I/O	CORE	N	N	3.3V	GPO	STRAPPED L
GPIO18	Unmultiplexed	AC20	I/O	CORE	N	N	3.3V	GPO	NC
GPIO19	SATA_1GP	AH18	I/O	CORE	N	N	3.3V	GPI	STRAPPED HI
GPIO20	Unmultiplexed	AF21	I/O	CORE	N	N	3.3V	GPO	NC
GPIO21	SATA_OGP	AF19	I/O	CORE	N	N	3.3V	GPI	STRAPPED HI
GPIO22	REQ4#	A13	I/O	CORE	N	N	3.3V	Native	STRAPPED HI
GPIO23	LDRQ_1#	AA5	I/O	CORE	N	N	3.3V	Native	STRAPPED HI
GPIO24	Unmultiplexed	R3	I/O	Resume	N	N	3.3V	GPO	NC
GPIO25	Unmultiplexed	D20	I/O	Resume	Y	N	3.3V	GPO	GPIO25(high 7507,low 7398)
GPIO26	Unmultiplexed	A21	I/O	Resume	N	N	3.3V	GPO	USB_EN
GPIO27	Unmultiplexed	B21	I/O	Resume	N	N	3.3V	GPO	NC
GPIO28	Unmultiplexed	E23	I/O	Resume	N	N	3.3V	GPO	NC
GPIO29	OC5#	C3	I/O	Resume	N	N	3.3V	GPI	USB_OCP#2
GPIO30	OC6#	A2	I/O	Resume	N	N	3.3V	GPI	USB_OCP#3
GPIO31	OC7#	B3	I/O	Resume	N	N	3.3V	GPI	USB_OCP#3
GPIO32	Unmultiplexed	AG18	I/O	CORE	N	N	3.3V	GPO	BIOS_WP#(fill with 1)
GPIO33	Unmultiplexed	AC19	I/O	CORE	N	N	3.3V	GPO	NC
GPIO34	Unmultiplexed	U2	I/O	CORE	N	N	3.3V	GPO	NC
GPIO35	SATACLKREQ#	AD21	I/O	CORE	N	N	3.3V	GPO	NC
GPIO36	SATA2GP	AH19	I/O	CORE	N	N	3.3V	GPI	STRAPPED HI
GPIO37	SATA3GP	AE19	I/O	CORE	N	N	3.3V	GPI	STRAPPED HI
GPIO38	Unmultiplexed	AD20	I/O	CORE	N	N	3.3V	GPI	STRAPPED HI
GPIO39	Unmultiplexed	AE20	I/O	CORE	N	N	3.3V	GPI	STRAPPED HI
GPIO48	GNT4#	A14	I/O	CORE	N	N	3.3V	Native	STRAPPED HI
GPIO49	CPUPWRGD	AG24	I/O	V_CPU_IO	N	N	V_CPU_IO	Native	H_PWRGD
Following are the GPIOs that need to be terminated properly if not used: GPIO[39:36,23:21,19,7:0]: default as inputs and should be pulled up to Vcc3_3 if unused. GPIO[31:29,15:8]: default as inputs and should be pulled up to VccSus3_3 if unused.									

SIO Fintek71882FG(CONTINUE)					
GPIO	Alt Func	PIN	Usage	Input/Output	NOTES
GPIO0	VIDOUT0	49	MCH_BSEL0	O12	
GPIO1	VIDOUT1	50	MCH_BSEL1	O12	
GPIO2	VIDOUT2	51	MCH_BSEL2	O12	
GPIO3	VIDOUT3	52	NC	O12	
GPIO4	VIDOUT4	53	NC	O12	
GPIO5	VIDOUT5/SIC	54	NC	I/OD12t	
GPIO6	SLOT0CC#	55	GPO	I/OD12t	
GPIO7	Turbo1#/WDTRST#	56	WDTRST#	OD12-5v	
GPIO15	LED_VSB/ALERT#	64	LED_VSB	OD12	
GPIO16	LED_VCC/Turbo2#	65	LED_VCC	OD12	
GPIO20	PCIRST1#	74	PCIRST1#	OD12	
GPIO21	PCIRST2#	75	PCIRST2#	O12	
GPIO22	PCIRST3#	76	PCIRST3#	O12	
GPIO23	RSTCON#	77	RSTCON#	OD12	
GPIO24	ATXPG_IN	78	ATXPG_IN	AIN	
GPIO32	PWROK	84	PWROK	OD12	
GPIO26	PWSIN#	80	PWSIN#	INts5v	
GPIO27	PWSOUT#	80	PWSOUT#	OD12	
GPIO30	S3#	82	S3#	INts5v	
GPIO31	PSON#	83	PSON#	OD12-5v	
GPIO33	RSMRST#	85	RSMRST#	OD12	
GPIO40	FANIN3	25	FANIN3	INts5v	
GPIO41	FAN_CTL3	26	FAN_CTL3(NC)	OD12-5v	
GPIO25	PME#	79	PME#	OD12-5v	
GPIO10	SPI_SLK/FANIN4	59	GPIO10(NC)	I/OD12t	
GPIO11	SPI_CS0#/FANCTL4	60	GPIO11(NC)	I/OD12t	
GPIO12	SPI_MISO/FANCTL1_1	61	GPIO12(NC)	I/OD12t	
GPIO13	SPI_MOSI/BEEP	62	BEEP(NC)	OD24	
GPIO14	FWH_DIS/WDTRST#/SPI_CS1#	63	GPIO14	I/OD12t	
GPIO42	IRTX	27	IRTX	O12	
GPIO43	IRRX	28	IRRX	INts	
GPIO17		66	NC	I/OD12t	

PCI Config.

DEVICE	MCP1	INT	PIN	REQ#/GNT#	IDSEL	CLOCK
PCI1	PIRQ#A				AD16	PCI_CLK0
	PIRQ#B					
	PIRQ#C					
PCI2	PIRQ#D				AD17	PCI_CLK1
	PIRQ#B					
	PIRQ#C					
	PIRQ#D					
	PIRQ#A					

JCI1	Chassis Intrusion
Open	Normal
(1-2)	Chassis Open

DDRII DIMM Config.

DEVICE	ADDRESS	CLOCK
DIMM A	A0H	P_DDR0_A/N_DDR0_A
		P_DDR1_A/N_DDR1_A
		P_DDR2_A/N_DDR2_A
DIMM B	A4H	P_DDR0_B/N_DDR0_B
		P_DDR1_B/N_DDR1_B
		P_DDR2_B/N_DDR2_B

JUMPER SETTING

JBAT1	(1-2)NORMAL	(2-3)CLEAR
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0A Change list:

- 1. Add DMI Audio net name
- 2. Change LED Power pull high to 680 Change r20 to 1.5K
- 3. Change D10 D11 Power pull VCC5, Q20 Pull up VCC3
- 4. Delet R252 R254 C132 R22 C60,change U5 to I95-7523212-T07
- 5. Modify footprint : C_P3_5_D8_H9 NC_0402_6 NC_0603_10 C0805MSB C0603MS_BOT
- 6. Swap RN65 RN61 RN23 RN64 RN63 RN24 RN28 RN25 RN66 ; Delet EC20,
- 7. Add 5VCC TO 3VCC sequence
- 8. change TESTPIN30 to TPC20B
- 9. RENAME ,Swap RN37, X_J1 Change to GND , Change C300 C301 to 0.22UF
- 10. Modify V_1P25_CORE to G31

1.0 Change list:

- 1. U11 EN(pin3)change to USB_DRV
- 2. Add SIO pin55 SKTOCC# pull up to 3vsb
- 3. Swap RN26
- 4. add Control UP7501 power sequence

7592 Change list:

- 1. modify G31 to G41; LAN=> TRL8111DL; ALC888 - > change to ALC888S VC2;
SIO: I/O Fintek 882 - > Change to 889;
LAN : 8111C /8101E > Change to 8111DL / 8101E ;
Vcore ST6703 > Change to UPI 6206 2008/10/13
- 2.reserved 0 ohm to GND for ALC888s pin4
change DDR to quar choke (ckhokel/2) 10/15
change Q27 to N7002 from 3904, change 2pcs N3904 to Q36 ;
chage LAN circuit => modify EL cap to MLCC for +3VSB; add 2n3904 for link100/1000 ;10/16
install copper to instand LXX :10/17
- 3. modify TPM footprint;=JLPC1_TPM 10/20
- 4. remove H/VSYNc to GND resistor, (only onboard VGA) 10/21
- 5:Pin 23 is GPO pin for8111DL. It is used forDSM function. 10/22
- 6. reserved SIO Peci_req# to ICH7 Bmbusy# 10/23
- 7. reserved ITPM die to resistor (G41 no support ITPM 10/23
- 8, delect零件子阶(零件子增) 10/24
- 9 ,reserved PSI function circuit, reserved PGNT#3 to Vcc3 for ICH Top Block-swap issue
- reserved LPC_DRQ#0 pull high resistor (ICH7 &SIO interpull high) 10/24
- 10. H_VCCPLL 与VCCDQ_CRT分开以免layout时被相互干扰 10/24
- 11.H_COMP4 reserved Pul up R(DEMO board reserved); ICH7 pinAF24/AH25 for desttop is test pint,
for mobile is DPRSTP#/DPSLP#=> 0 ohm R to ICH7 no stuff , stuff CPU side pull high R to VTT; 10/26
- 12. PCIE slot footprint chage to SLOT_PCIEXP164_2(耳扣向上往CPU方向)
Clock part: cange 2 pcs 3904 to 1 2n3904 for layout size;10/27
- 13. reserved a DDR DIMM input EL cap ;
change VRM part some RC to 0603 footprint, reserved a SP_cap10/28
- 14. remove some NB TXX(test pad) for layout , 10/30
- 15: reserved RNXX for HDMI (RNXX intershort) P8; del TPM CONN TPMCLK 10P EMI cap; SWap RN64 .6&8 (CPUSEL2) 10/31
- 16: Swap RN15.1&3 , update NB_sink/EC36/37/R380 tol CIS library 11/03
- 17, modify some 0805 to 0603 cap for layout and reserved 1.1_core cap for cost (p8) ; change H/VSYNc_1 location for cost; 11/04
- 18: update NB ci library; change Audio 100uf cap to EL cap 11/05
- 19: modify test point footprint from tcp20B to testpin25
change VRM CS1/2/3+ to 1.5K ohm, reserved C8; 11/06
- 20 PLTRST_BU1# pull high from 220 ohm to 1K (VCC3) ==test signal 11/07
- 21: reservec SATALED# & AC_RST# pull high resistor 11/08
- 22 Footprint update: OSCC_MS 为 N_OSCC_MS 11/10
- add rubber 6010: P/N:E25-7530010-C81 11/12
- 23 R40/R41 change 0402 value 11/21

7592 1.0 Change list:

- 1. SIO Version:B change to Version: C; SIO pin99(VCC) modify to 3VSB, pwok(pin80) modify to 3VSB ;
DMI CAP change to 0510 for SMT process ; update LAN_usb footprint, R181 for 8111DL, 8103E no install;1202
- 2> modify NB core and NB_sink P/N ;c211 change to 0603;C359 chage to 3vsb for SIO Pin99 from Vcc3;
R158 R160 place NB side for SI bug;; add R486 for intel seq; 1212

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History			
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